

***PHRAA***

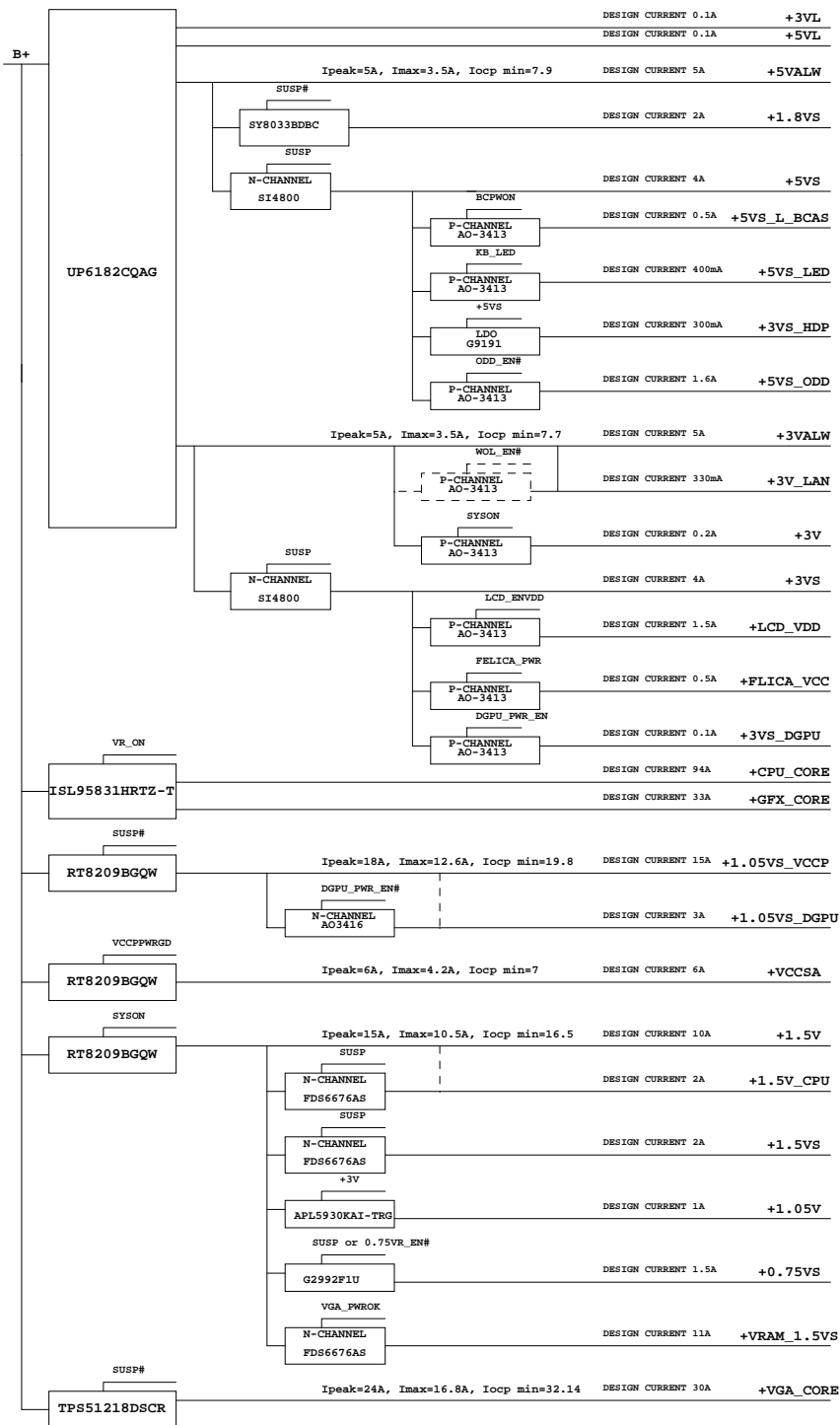
***Superior 10/10G***

# LA-7211P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)  
2011-01-31 Rev 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	<b>SCHEMATIC, MB A7211</b>
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Size B	Document Number <b>4019BD</b>
				Date Monday, February 28, 2011	Rev B
				Sheet 1	of 59





Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	3 of 69

## Voltage Rails

( O MEANS ON X MEANS OFF )

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

## PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

## EC SM Bus1 Address

## EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	NVIDIA GPU	9A H	1001 1010 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

## BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

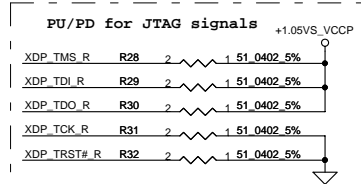
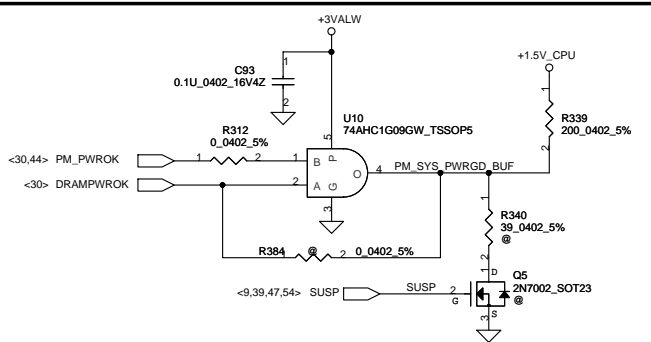
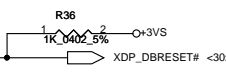
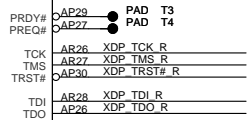
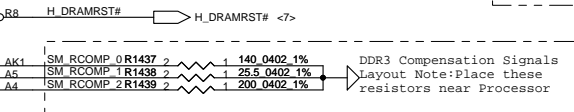
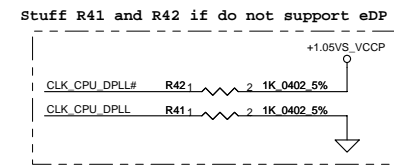
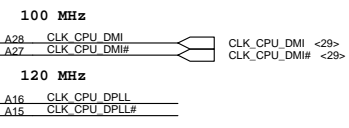
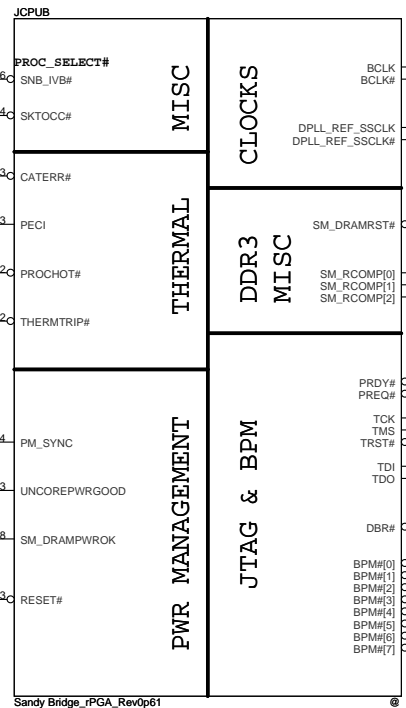
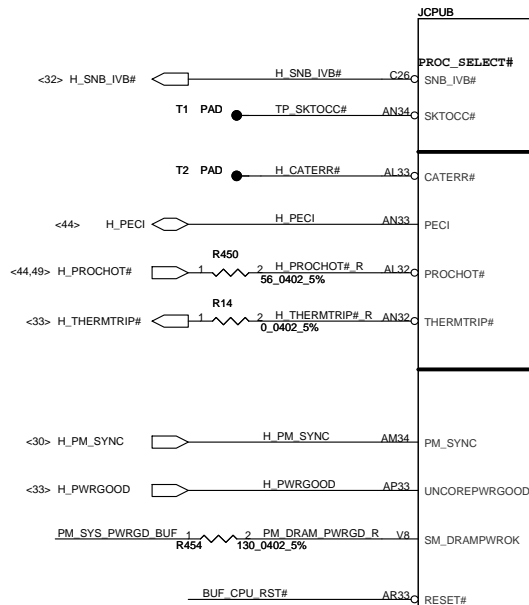
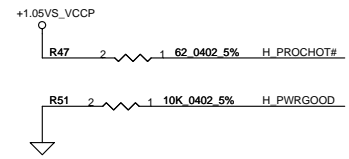
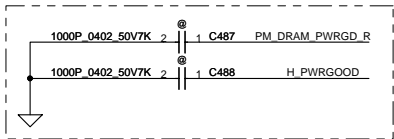
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

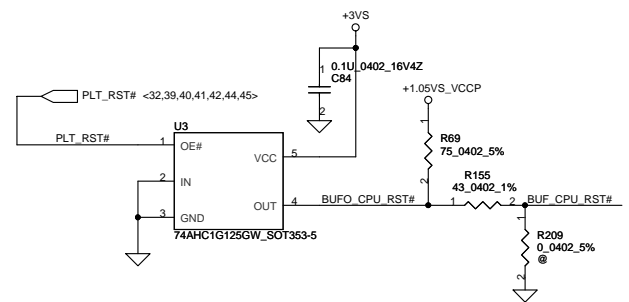
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

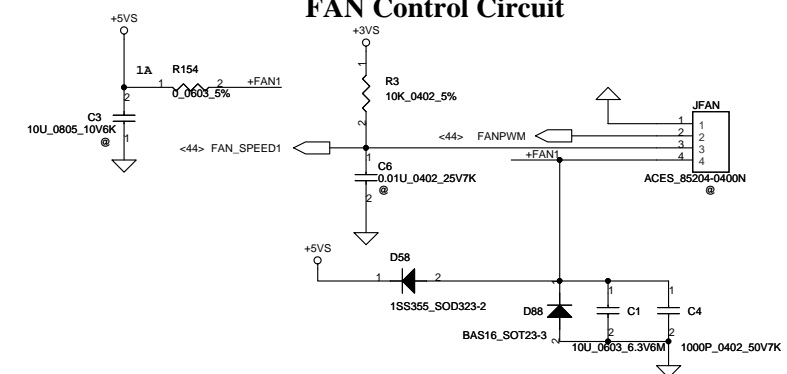
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/01/31		Deciphered Date		2012/12/31		Title	
								SCHEMATIC, MB A7211	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.									
						Document Number		4019BD	
						Date:		Monday, February 28, 2011	
						Sheet		4 of 59	



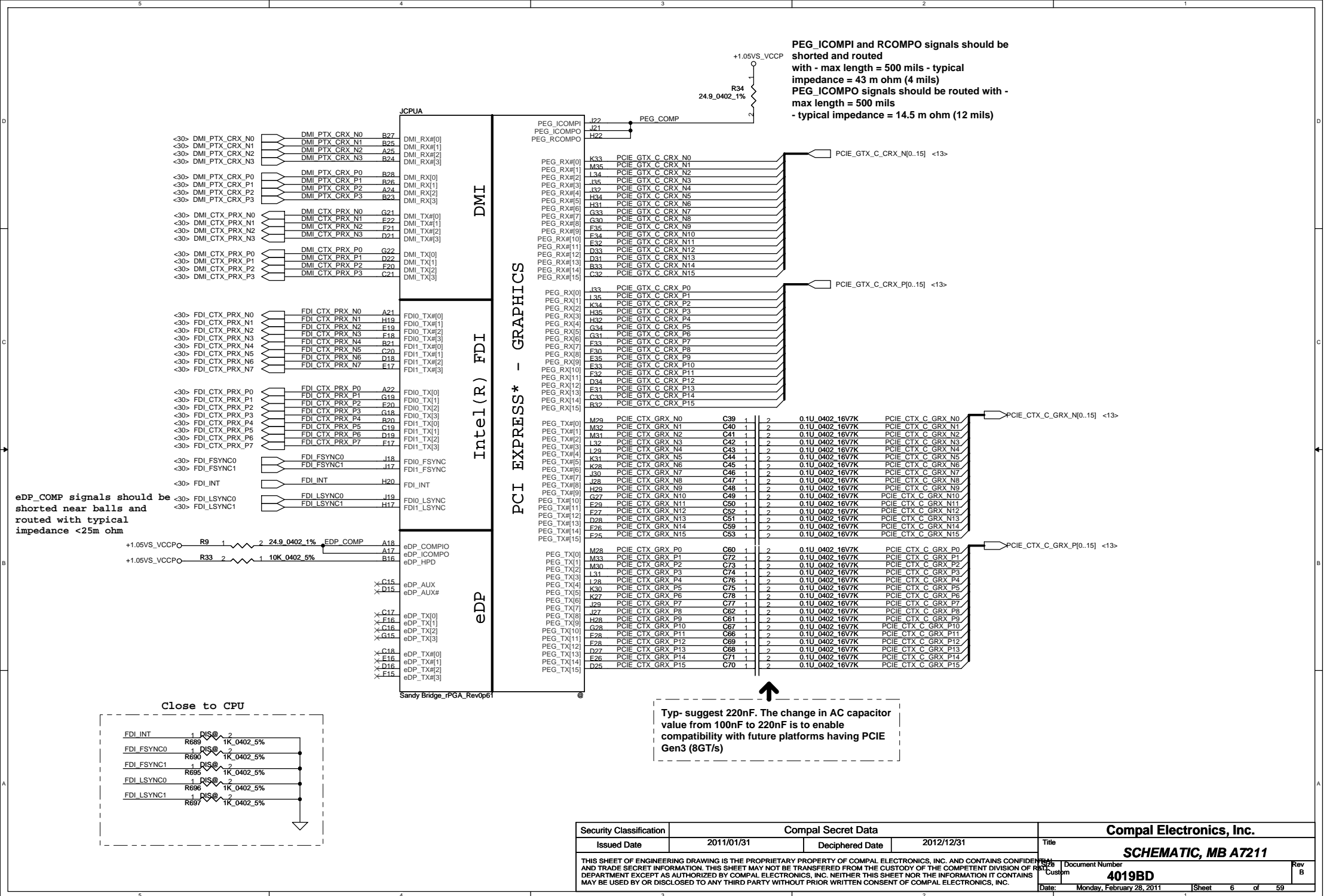
Buffered Reset to CPU



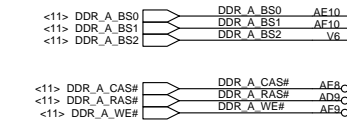
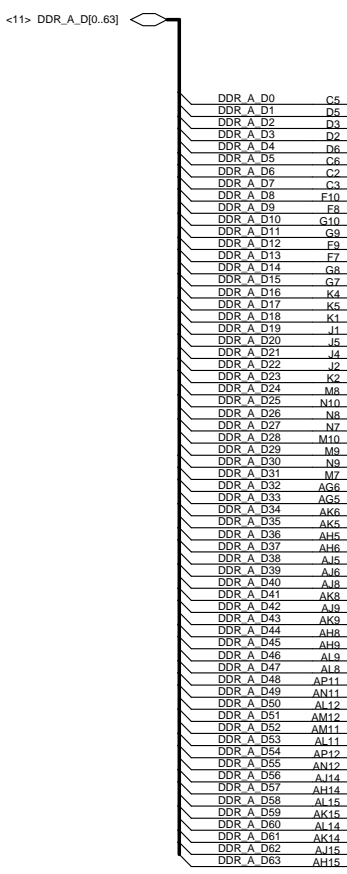
FAN Control Circuit



Security Classification	Compal Secret Data			Title	Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Document Number	SCHEMATIC, MB A7211	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Customer	4019BD	Rev B
Date:	Monday, February 28, 2011	Sheet	5 of 59			

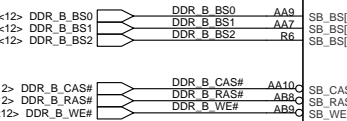
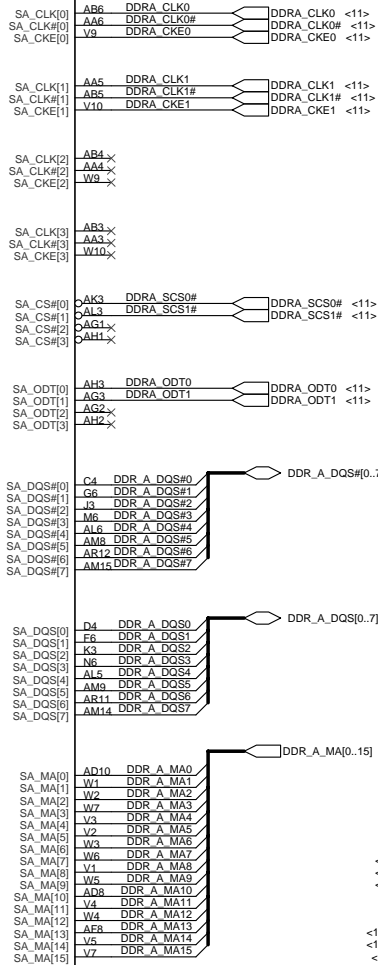


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	6 of 59



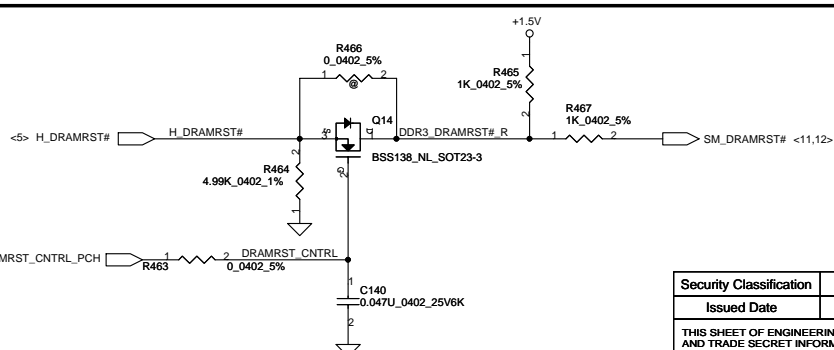
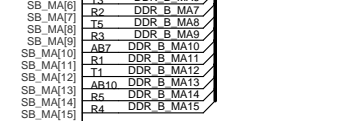
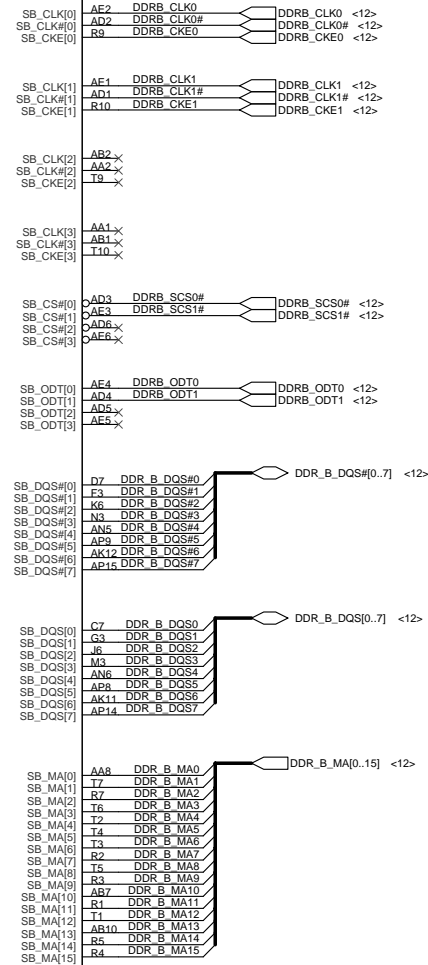
Sandy Bridge\_rPGA\_Rev0p61

# DDR SYSTEM MEMORY A



Sandy Bridge\_rPGA\_Rev0p61

# DDR SYSTEM MEMORY B



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SCHEMATIC, MB A7211	
				Document Number	Rev B
				4019BD	
				Date: Monday, February 28, 2011	Sheet 7 of 59

+CPU\_CORE

## POWER

94A (Quad Core 45W)  
53A (SV 35W)

8.5A

PEG AND DDR

CORE SUPPLY

SVID

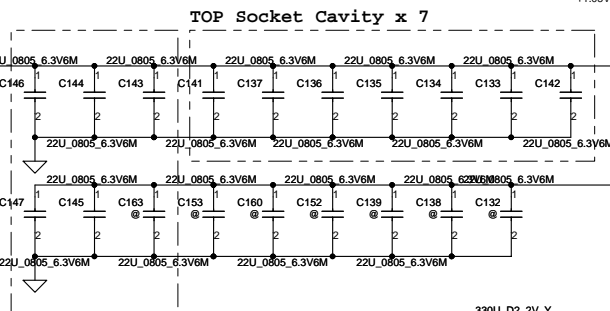
SENSE LINES

VCCIO1  
VCCIO2  
VCCIO3  
VCCIO4  
VCCIO5  
VCCIO6  
VCCIO7  
VCCIO8  
VCCIO9  
VCCIO10  
VCCIO11  
VCCIO12  
VCCIO13  
VCCIO14  
VCCIO15  
VCCIO16  
VCCIO17  
VCCIO18  
VCCIO19  
VCCIO20  
VCCIO21  
VCCIO22  
VCCIO23  
VCCIO24  
VCCIO25  
VCCIO26  
VCCIO27  
VCCIO28  
VCCIO29  
VCCIO30  
VCCIO31  
VCCIO32  
VCCIO33  
VCCIO34  
VCCIO35  
VCCIO36  
VCCIO37  
VCCIO38  
VCCIO39  
VCCIO40  
VCCIO41  
VCCIO42  
VCCIO43  
VCCIO44  
VCCIO45  
VCCIO46  
VCCIO47  
VCCIO48  
VCCIO49  
VCCIO50  
VCCIO51  
VCCIO52  
VCCIO53  
VCCIO54  
VCCIO55  
VCCIO56  
VCCIO57  
VCCIO58  
VCCIO59  
VCCIO60  
VCCIO61  
VCCIO62  
VCCIO63  
VCCIO64  
VCCIO65  
VCCIO66  
VCCIO67  
VCCIO68  
VCCIO69  
VCCIO70  
VCCIO71  
VCCIO72  
VCCIO73  
VCCIO74  
VCCIO75  
VCCIO76  
VCCIO77  
VCCIO78  
VCCIO79  
VCCIO80  
VCCIO81  
VCCIO82  
VCCIO83  
VCCIO84  
VCCIO85  
VCCIO86  
VCCIO87  
VCCIO88  
VCCIO89  
VCCIO90  
VCCIO91  
VCCIO92  
VCCIO93  
VCCIO94  
VCCIO95  
VCCIO96  
VCCIO97  
VCCIO98  
VCCIO99  
VCCIO100

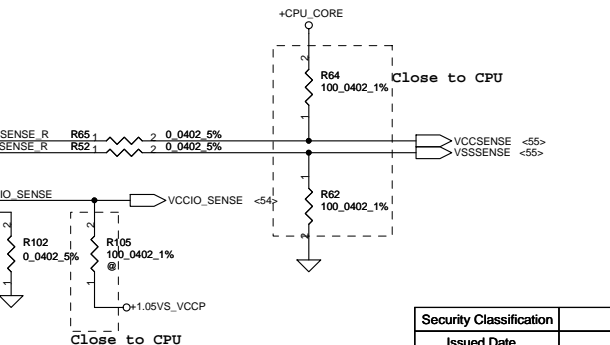
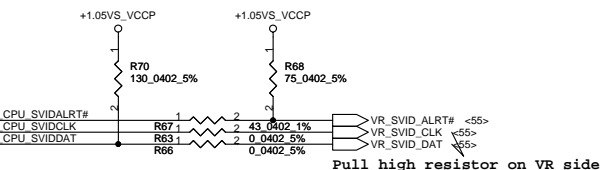
VIDALERT#  
VIDSClk  
VIDSOUT

VCC\_SENSE  
VSS\_SENSE

VCCIO\_SENSE  
VSSIO\_SENSE



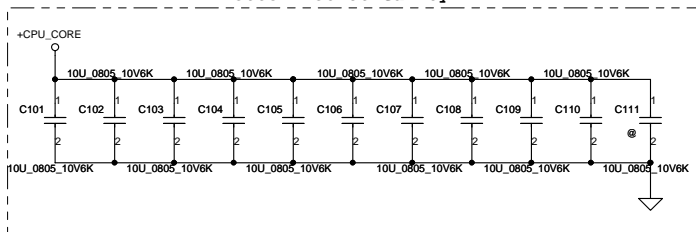
Bottom Socket Cavity x 5



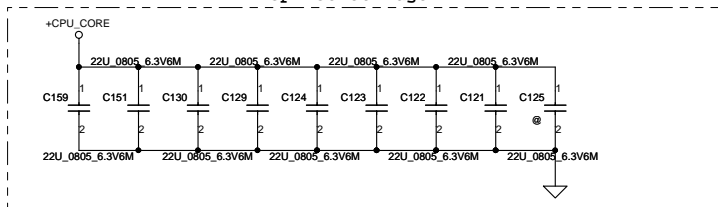
+1.05VS\_VCCP Decoupling:  
2X 330U (6m ohm), 12X 22U

+CPU\_CORE Decoupling:  
4X 470U (4m ohm), 16X 22U, 10X 10U

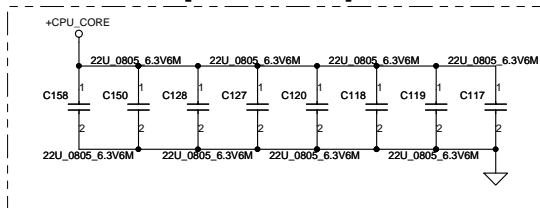
Bottom Socket Cavity



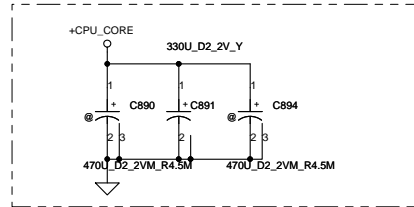
Top Socket Edge



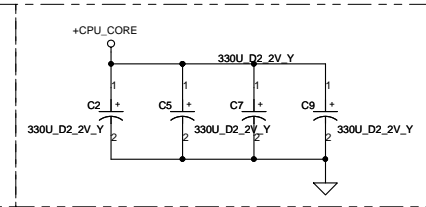
Top Socket Cavity



Co-Lay with C2, C5, C7, C9



TOP Socket Edge



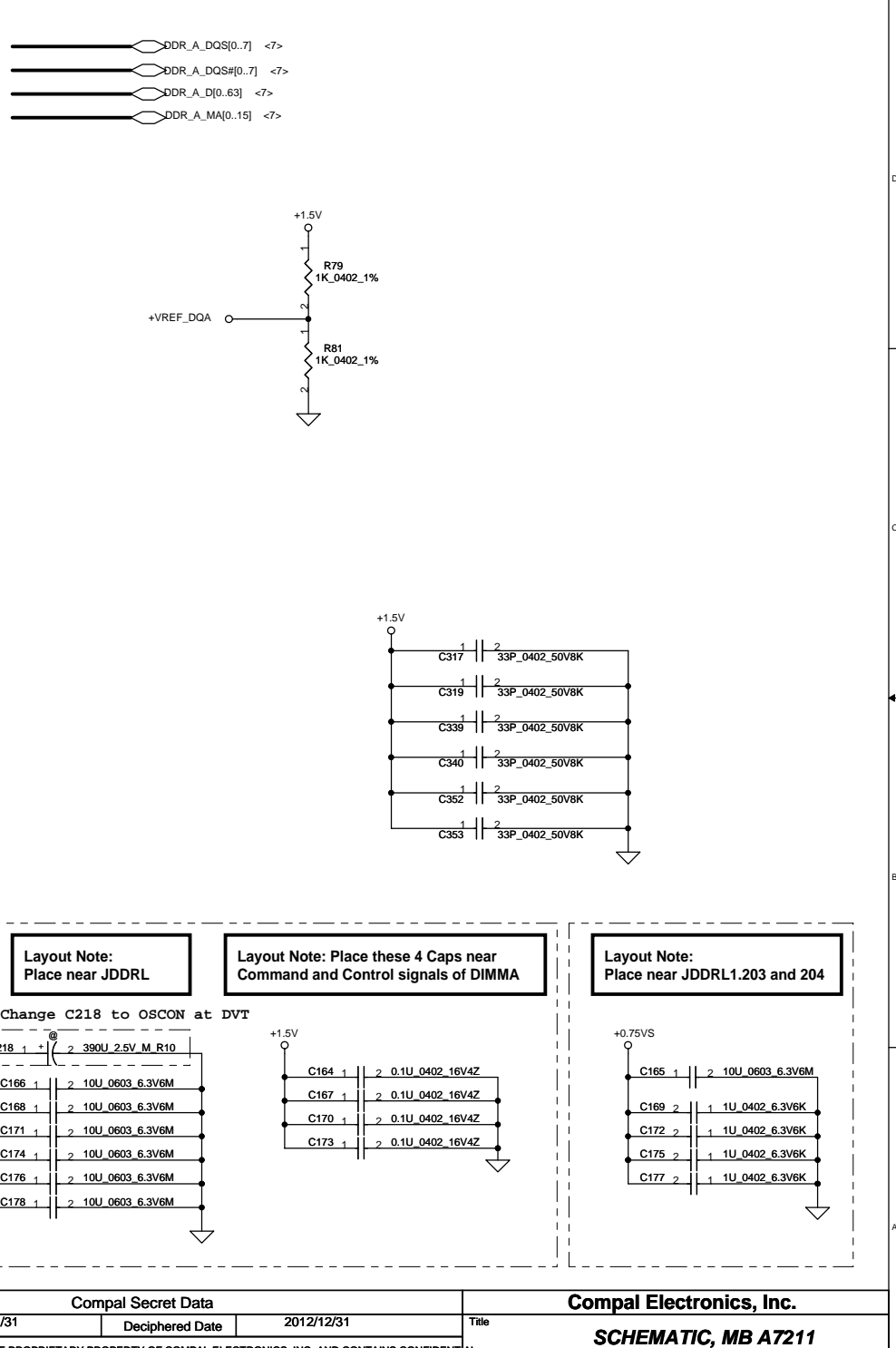
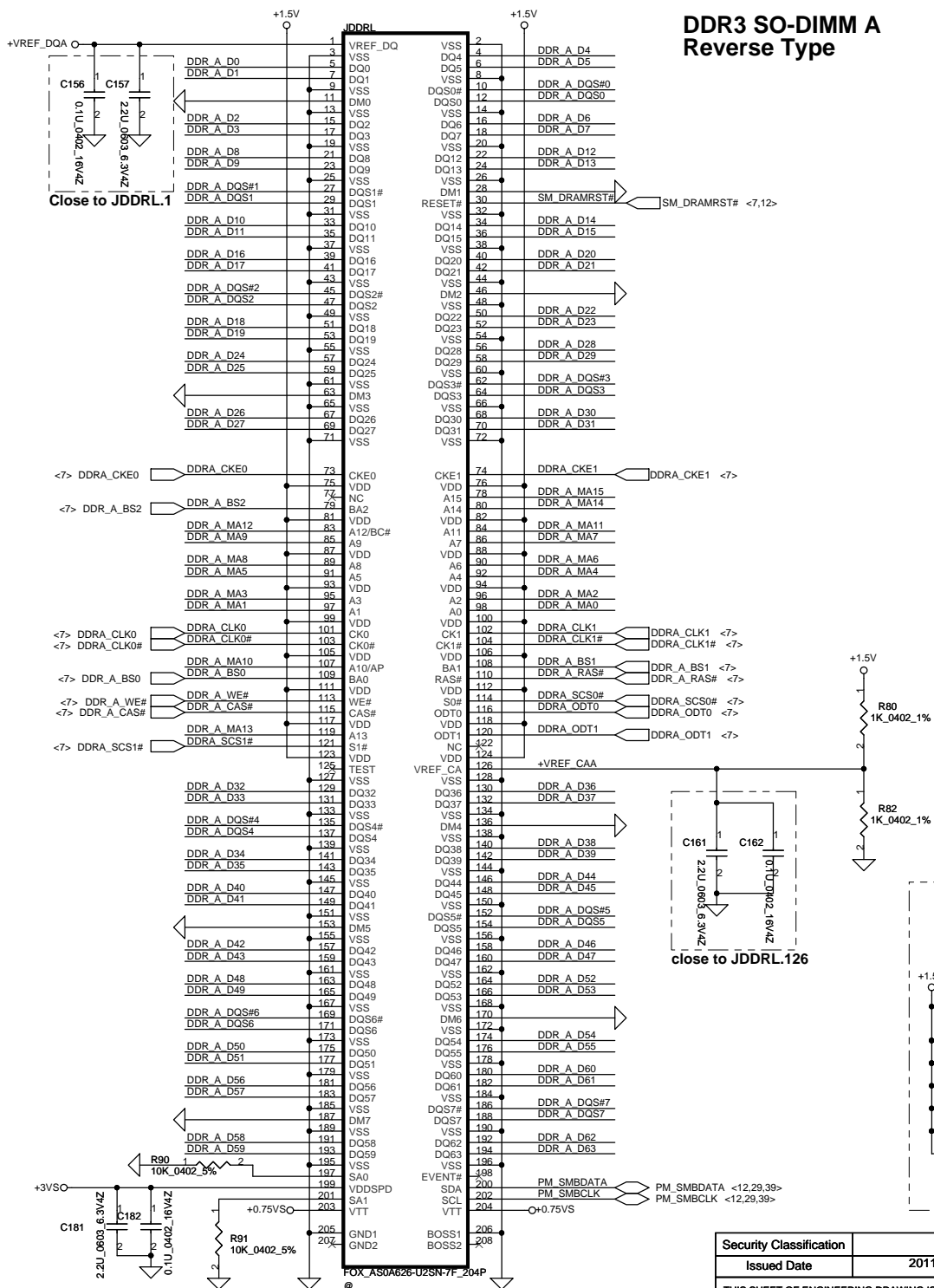
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number 4019BD
				Date	Monday, February 28, 2011
				Sheet	8 of 59



Title		<b>SCHEMATIC, MB A7211</b>	
Size	Document Number	Rev	
Custom	<b>4019BD</b>	B	
Date:	Monday, February 28, 2011	Sheet	9 of 59

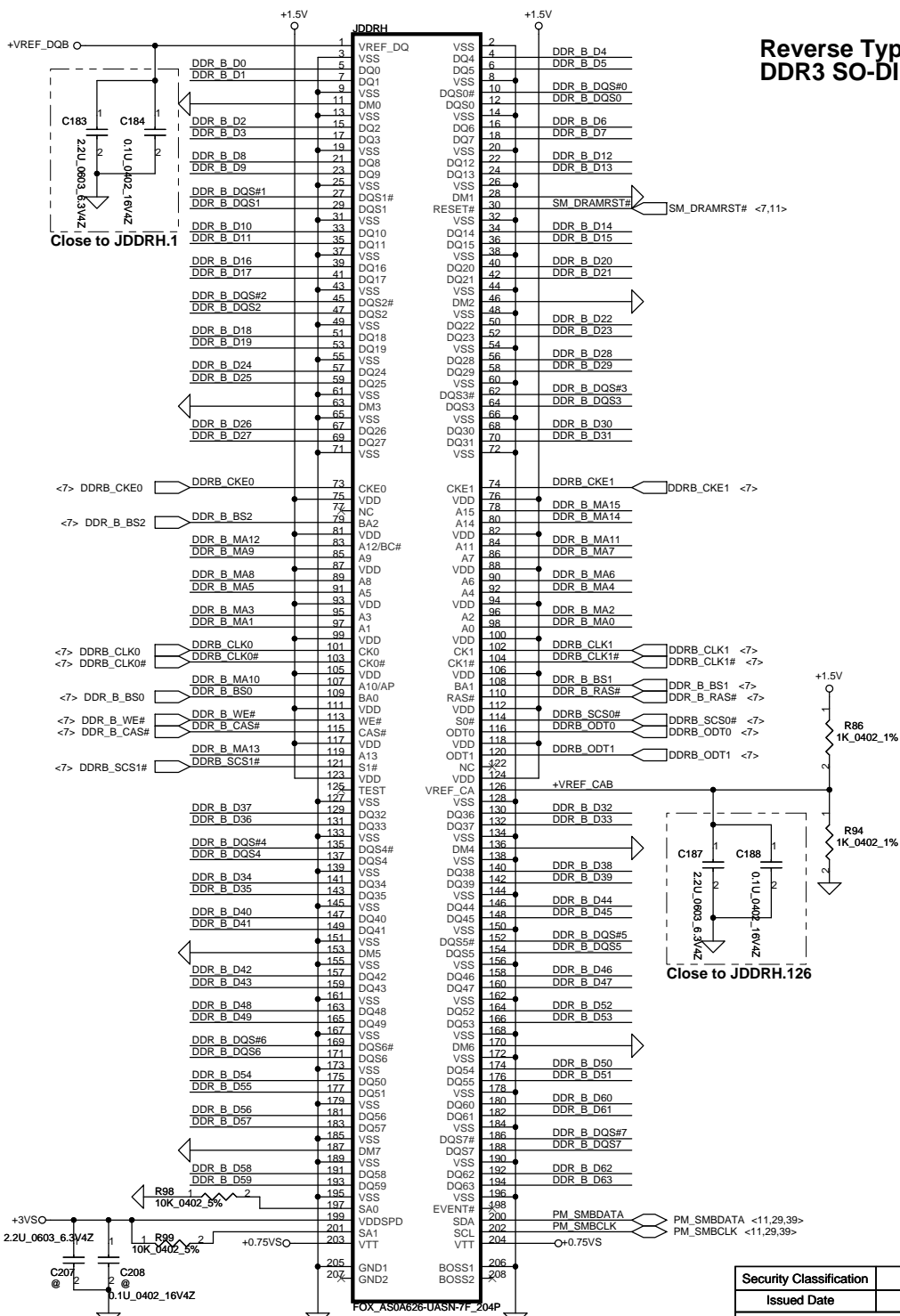


# DDR3 SO-DIMM A Reverse Type

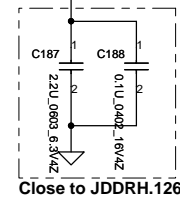
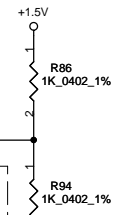
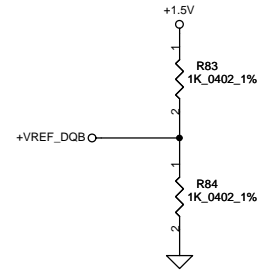


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document Number	B
				4019BD	
				Date	Monday, February 28, 2011
				Sheet	11 of 59

# Reverse Type DDR3 SO-DIMM B



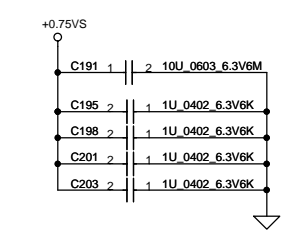
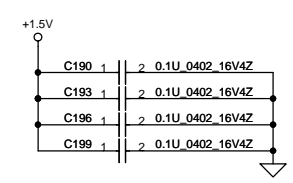
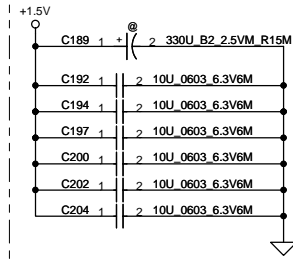
DDR\_B\_DQS#[0..7] <7>  
 DDR\_B\_DQS[0..7] <7>  
 DDR\_B\_D[0..63] <7>  
 DDR\_B\_MA[0..15] <7>



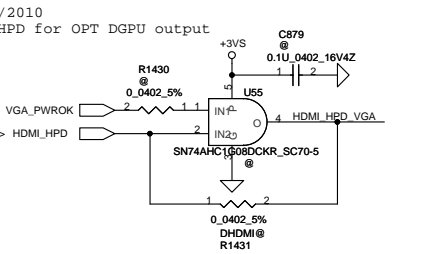
**Layout Note:**  
Place near JDDR.H

**Layout Note:** Place these 4 Caps near  
Command and Control signals of DIMMB

**Layout Note:**  
Place near JDDR.H.203 and 204



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SCHEMATIC, MB A7211	
				Size	Document Number
				Custom	4019BD
				Date	Monday, February 28, 2011
				Sheet	12 of 59



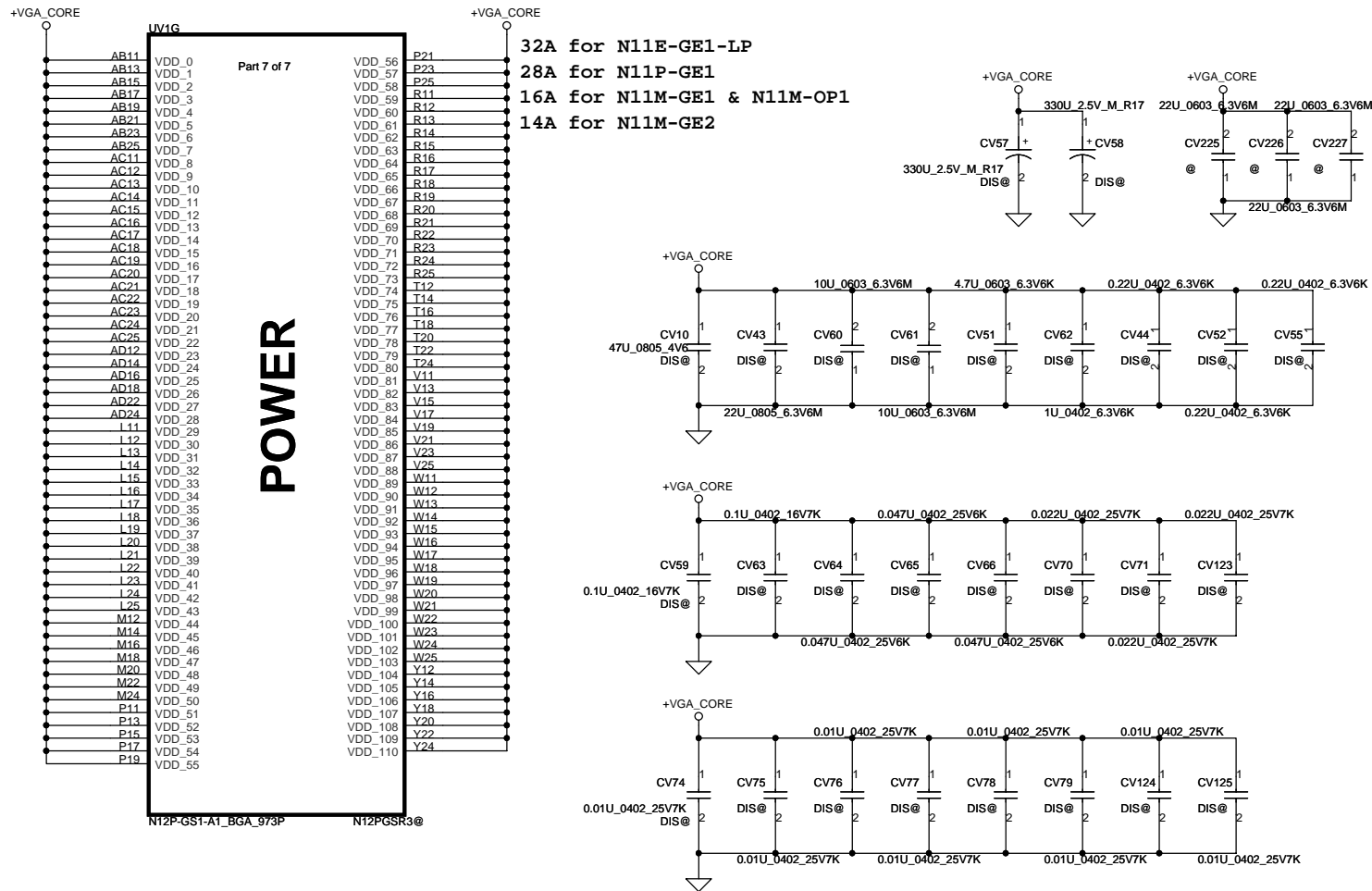


For PHQAA EVT Phase only			
Mode	VID1	VID0	+VGA_CORE
P0(Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

N12M-GE Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

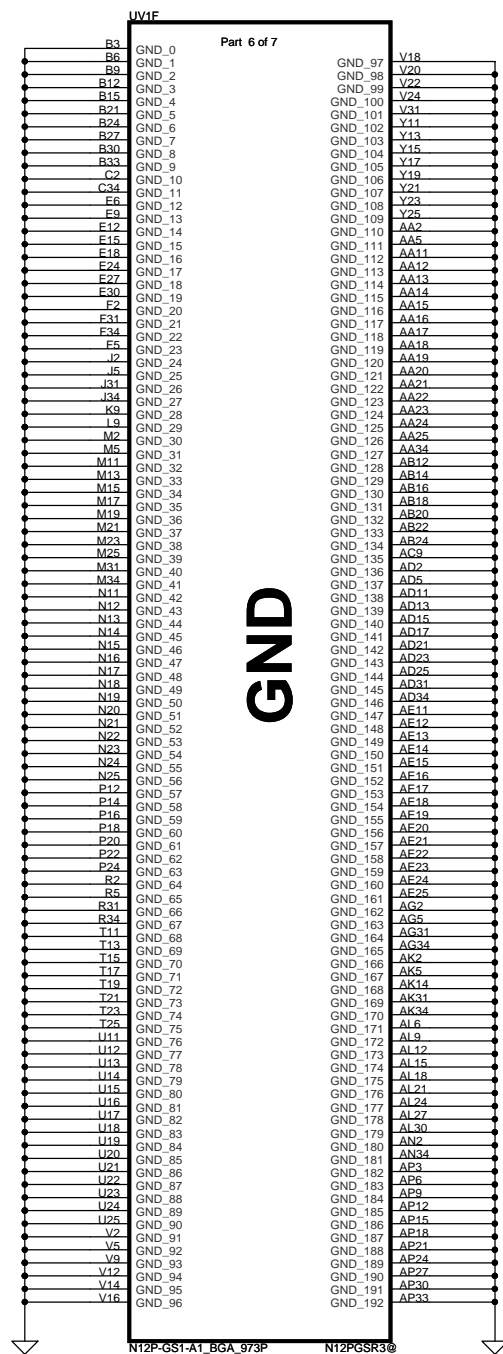
N12P-GS Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GE Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

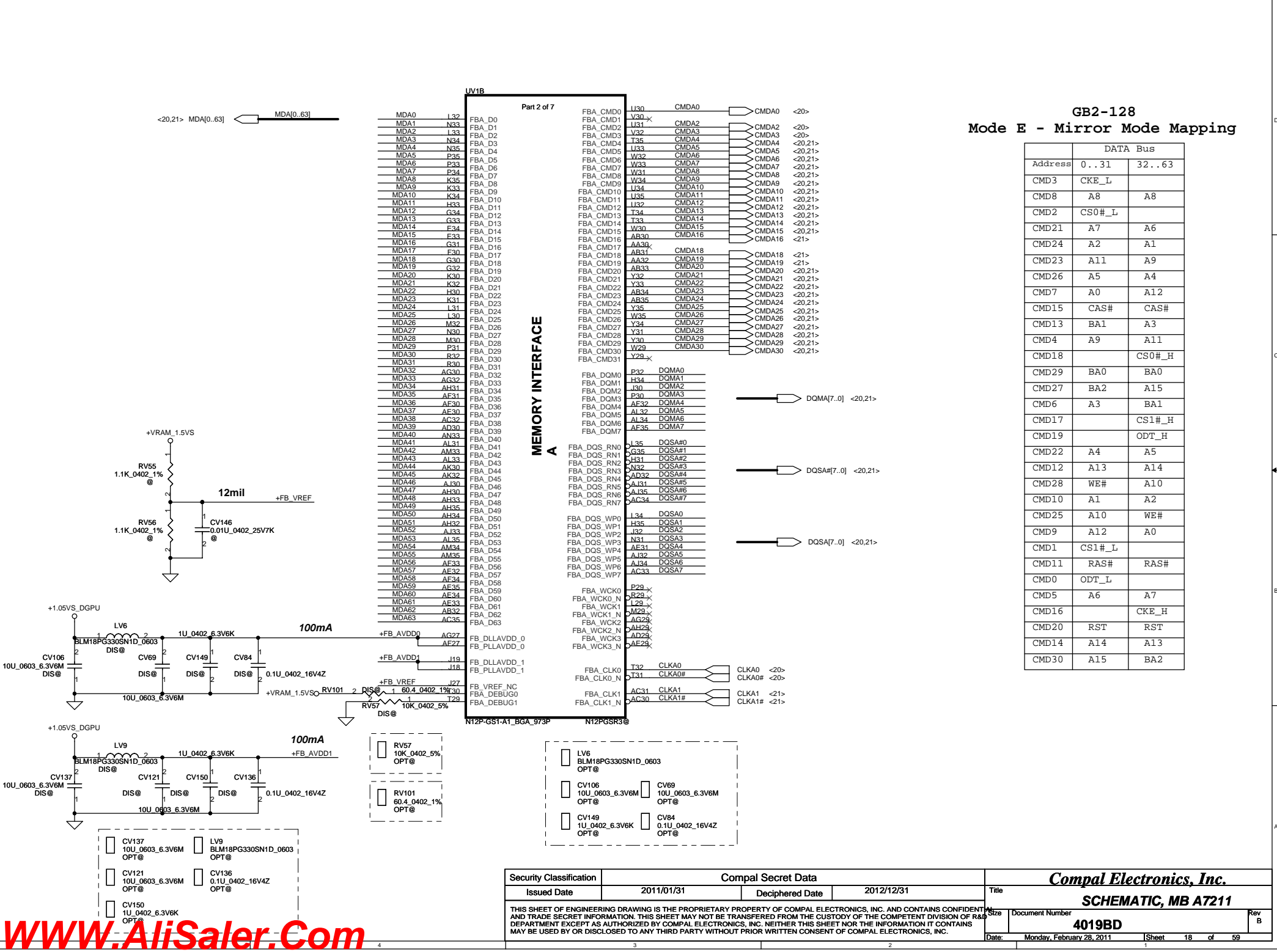








Security Classification		Compal Secret Data		Title	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	SCHEMATIC, MB A7211	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				4019BD	
				Date:	Monday, February 28, 2011
				Sheet	17 of 59



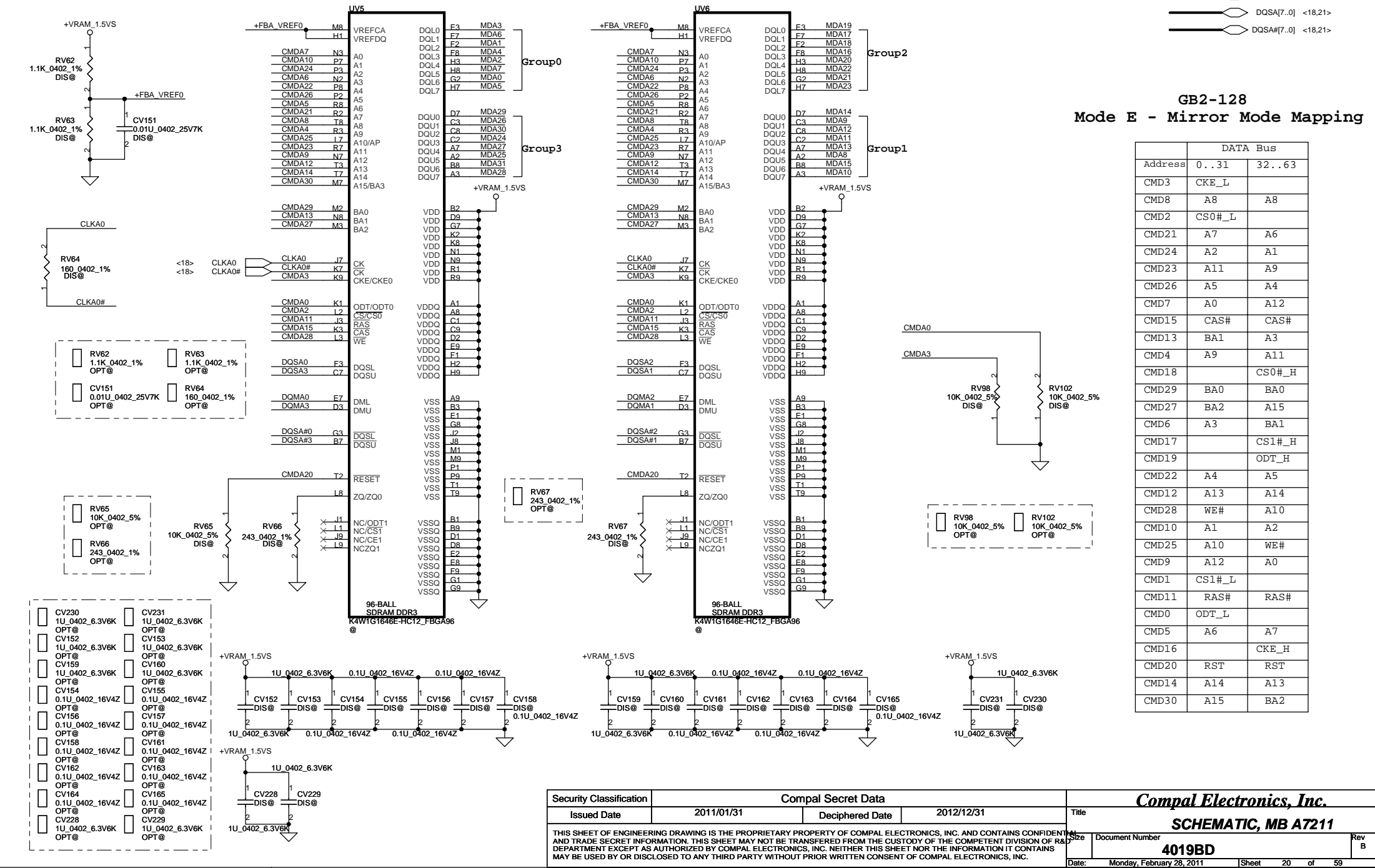
GB2-128  
Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

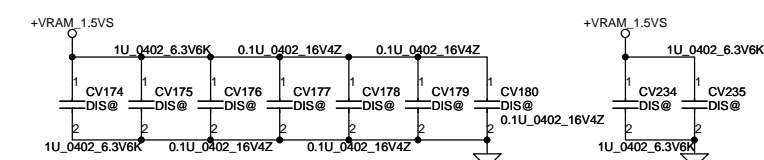
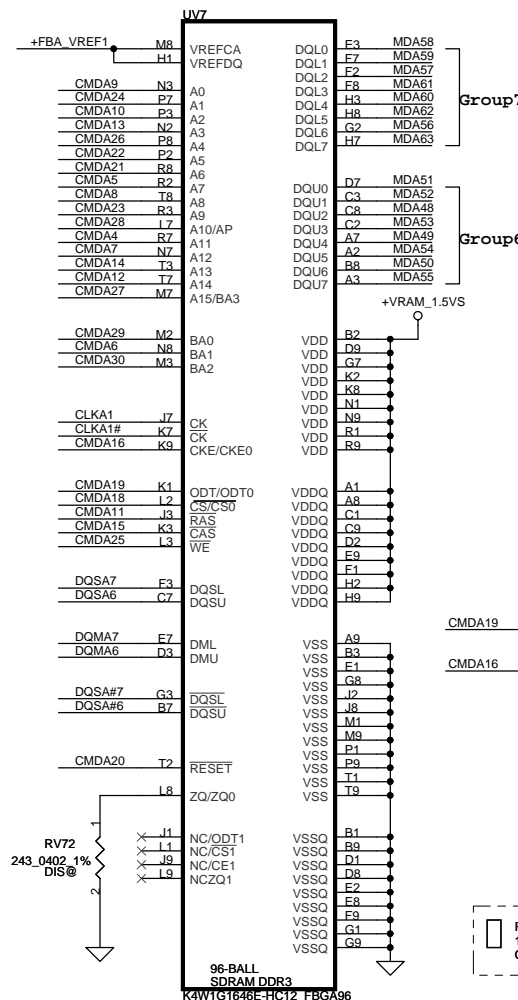
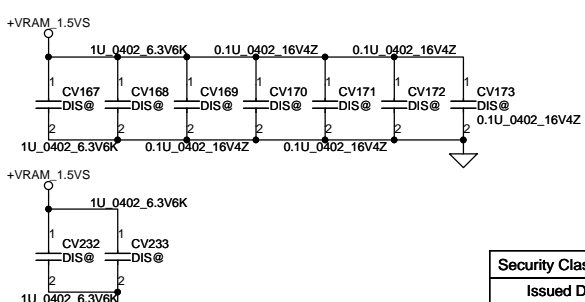
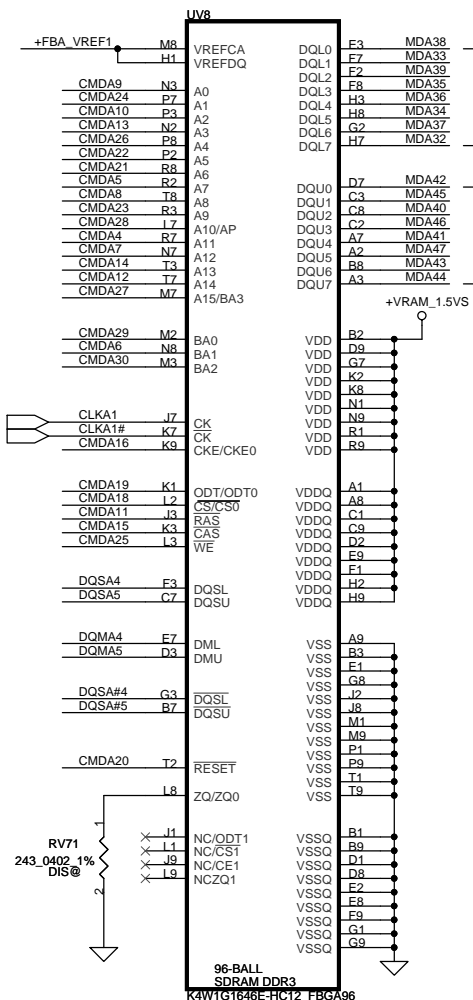
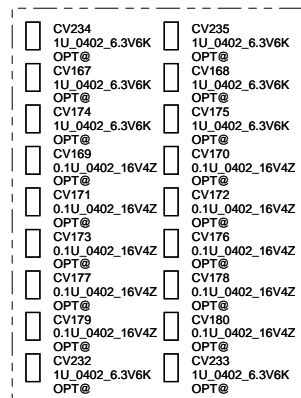
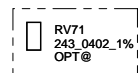
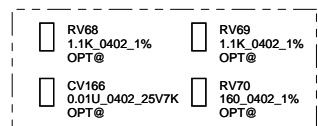
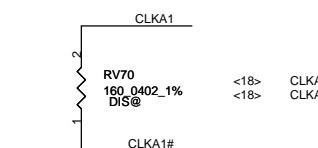
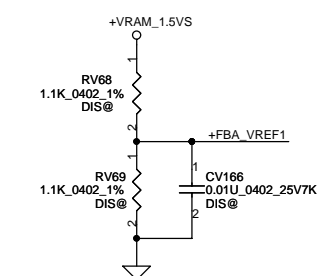
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				4019BD	
				Date	Monday, February 28, 2011
				Sheet	18 of 59



Memory Partition A - Lower 32 bits



## Memory Partition A - Upper 32 bits

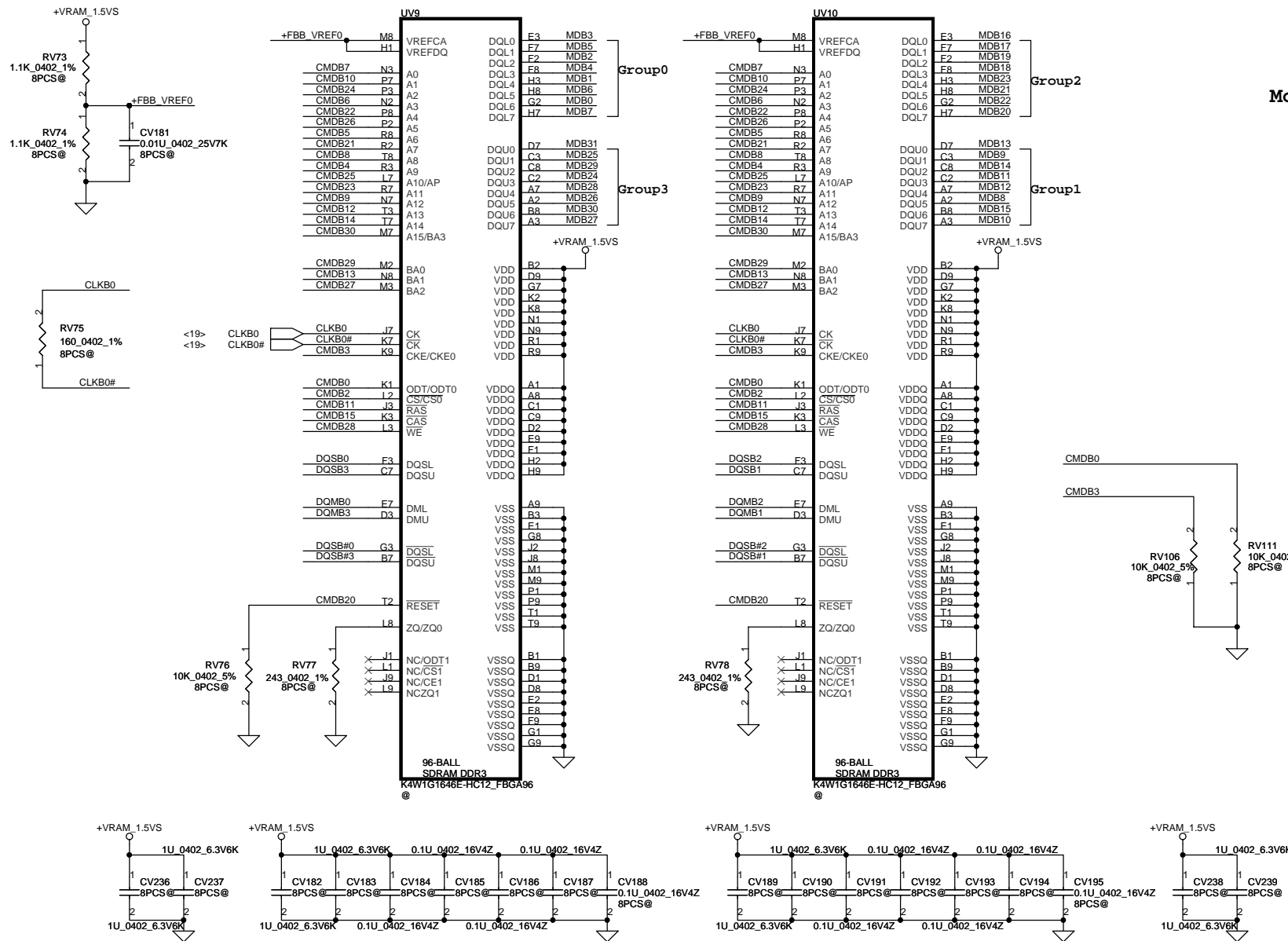


GB2-128  
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0...31	32...63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	<b>SCHEMATIC, MB A7211</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev B
					<b>4019BD</b>	
				Date:	Monday, February 26, 2011	Sheet 21 of 59

# Memory Partition C - Lower 32 bits



MDB[0..63] <19,23>  
 CMDB[30..0] <19,23>  
 DQMB[7..0] <19,23>  
 DQSB[7..0] <19,23>  
 DQSB#[7..0] <19,23>

**GB2-128**  
**Mode E - Mirror Mode Mapping**

DATA Bus		
Address	0..31	32..63
CMD8	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

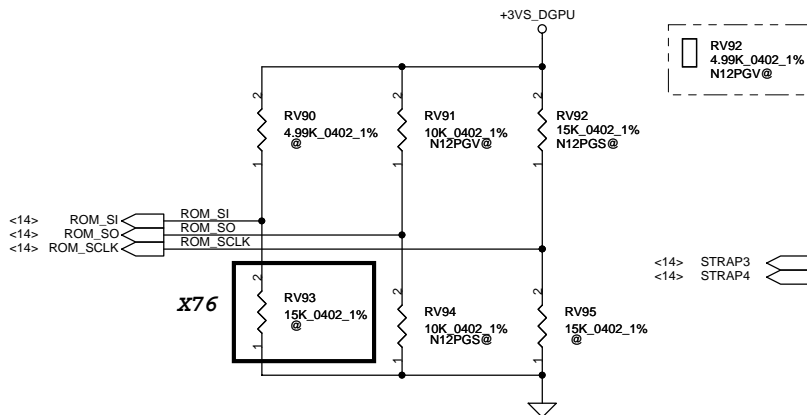
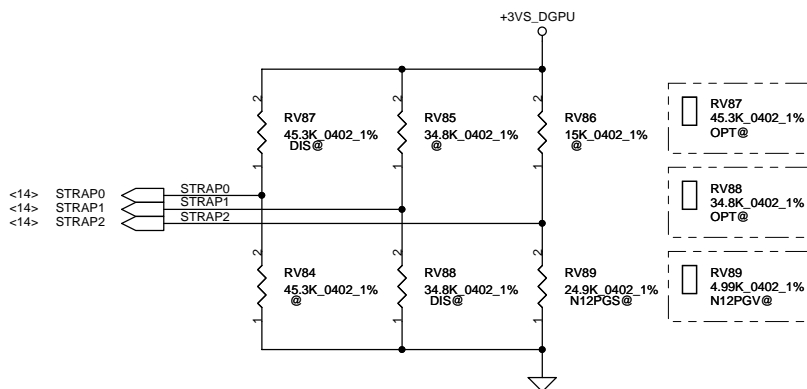
Security Classification		Compal Secret Data		Title	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	SCHEMATIC, MB A7211	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	22 of 59

## A



A

AA



GPU	DDR3 Type	VRAM	RAMCFG[3..0]	RV93
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C	512MB 0010	PD 15K SD034154280
		SA000041S20	1GB 0010	PD 15K SD034154280
		Samsung K4W1G1646E-HC11	512MB 0011	PD 20K SD034200280
		SA000041T00	1GB 0011	PD 20K SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C	1GB 0110	PD 34.8K SD034348280
		SA00003YO00	2GB 0110	PD 34.8K SD034348280
		Samsung K4W2G1646C-HC11	1GB 0111	PD 45.3K SD034453280
		SA000047Q00	2GB 0111	PD 45.3K SD034453280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C	512MB 0010	PD 15K SD034154280
		SA0000324C0		
		Samsung K4W1G1646G-BC12	512MB 0011	PD 20K SD034200280
		SA00004HS00		
	128M16 800MHz	Hynix H5TQ2G63BFR-12C	1GB 0110	PD 34.8K SD034348280
		SA00003VS00		
		Samsung K4W2G1646C-HC12	1GB 0111	PD 45.3K SD034453280

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

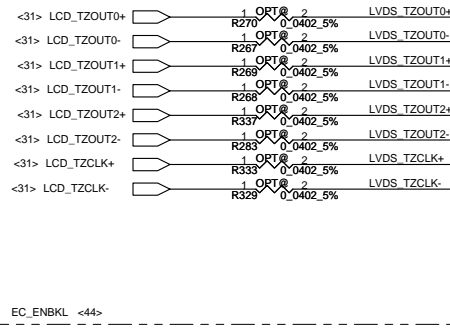
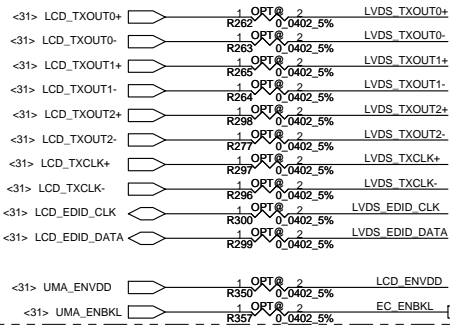
GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x1050	Pull up 15K	Pull down 5K

SUB_VENDOR		XCLK_417	
0	No VBIOS ROM (Default)	0	277MHz (Default)
1	BIOS ROM is present	1	Reserved
FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User[3:0]	
1	Reserved	1000-1100	Customer defined
3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
0110	Notebook Default	1	Enable
SLOT_CLOCK_CFG			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	24 of 59

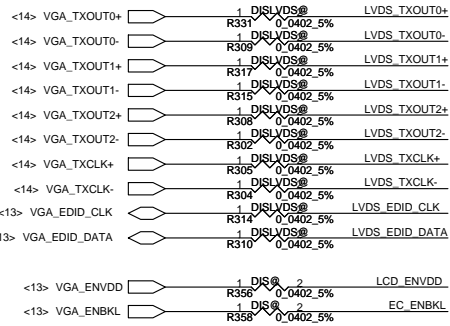


## OPTIMUS



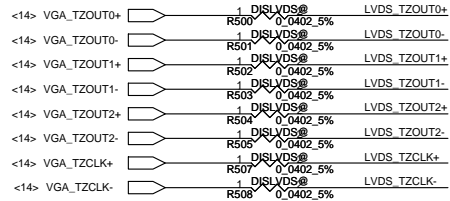
## Close to LVDS Connector

### DISCRETE



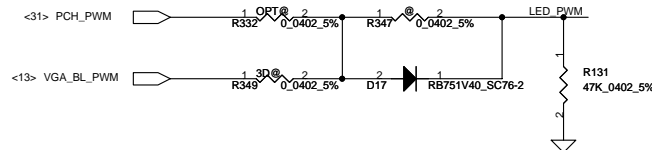
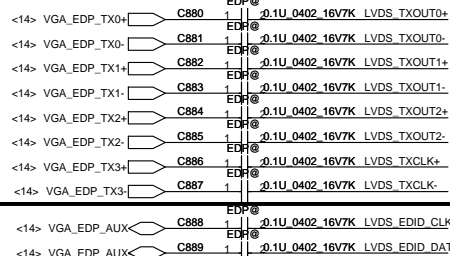
## Close to LVDS Connector

### DISCRETE for Dual Channel Panel



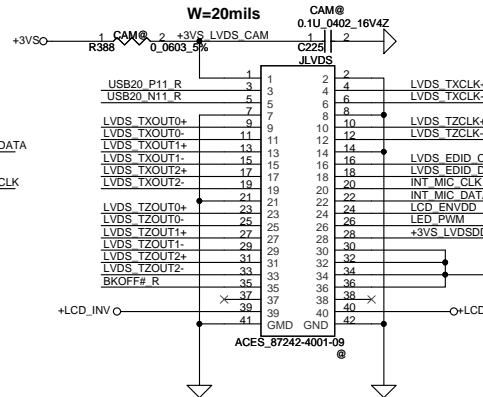
## Close to LVDS1 Connector

### DISCRETE for Full-HD and 3D eDP Panel

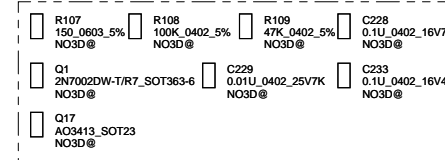
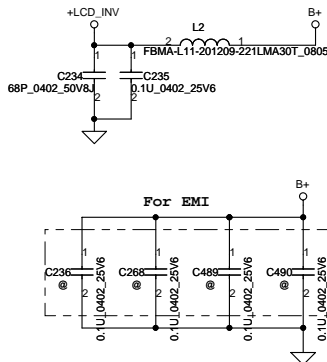
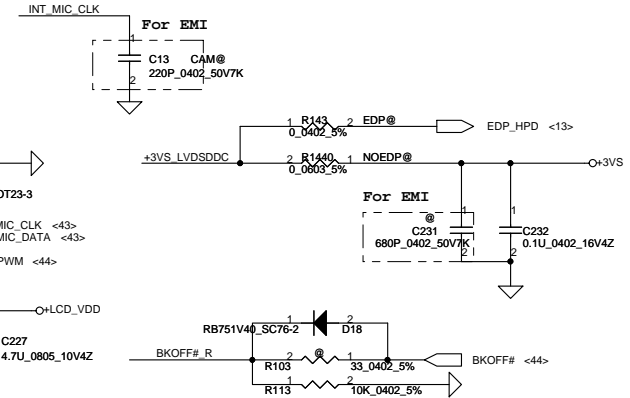
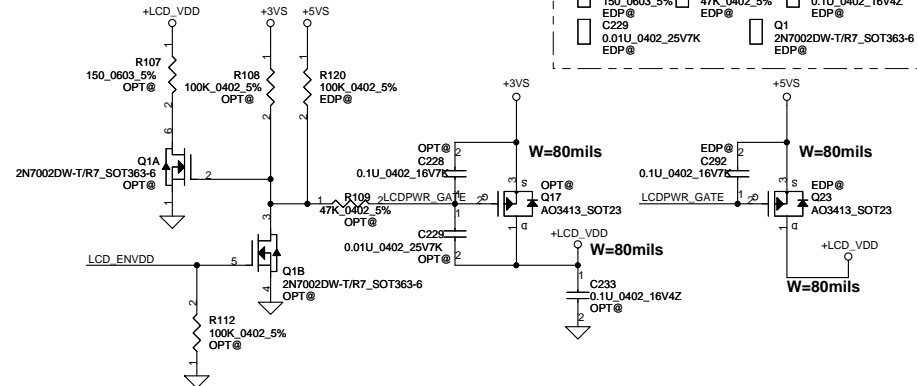
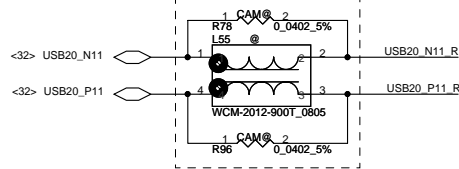


## Close to LVDS Connector

## LCD/PANEL BD. Conn.



### Reserve for EMI request



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SCHEMATIC, MB A7211		
				Size	Document Number	Rev
				Custm	40198D	B
				Date:	Monday, February 28, 2011	Sheet 25 of 59

## OPTIMUS

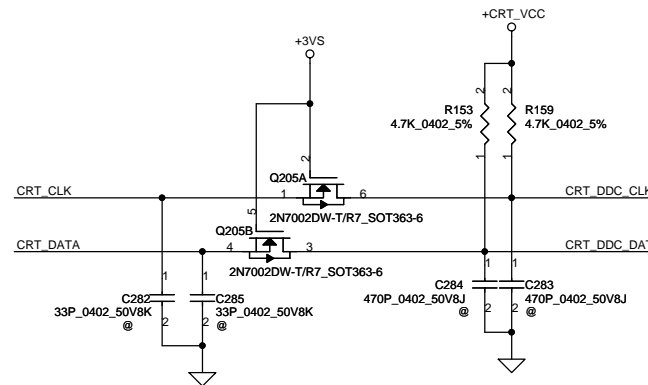
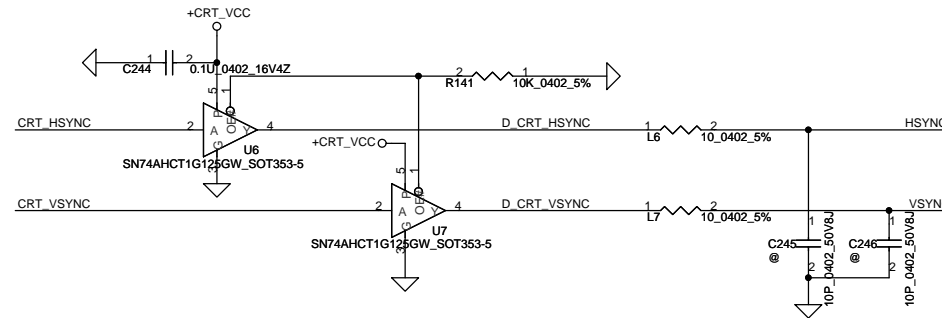
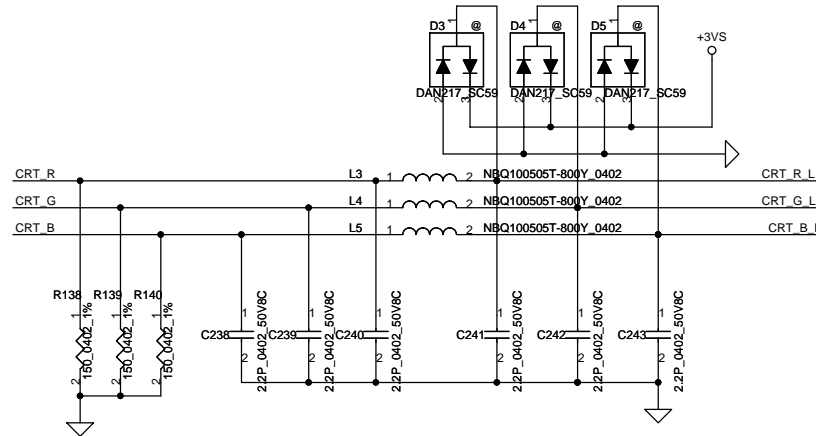
<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

Close to CRT Connector

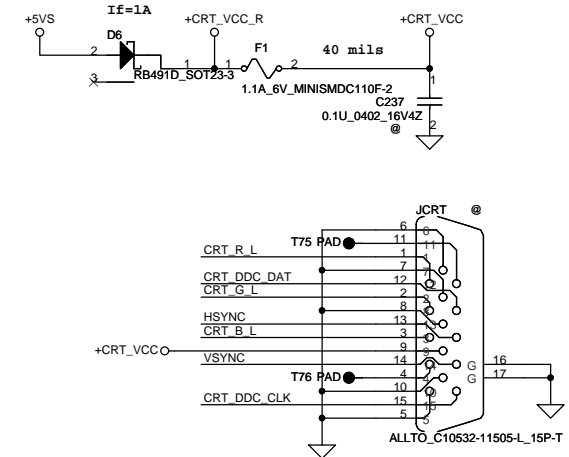
## DISCRETE

<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector

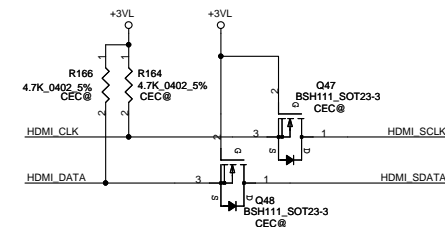
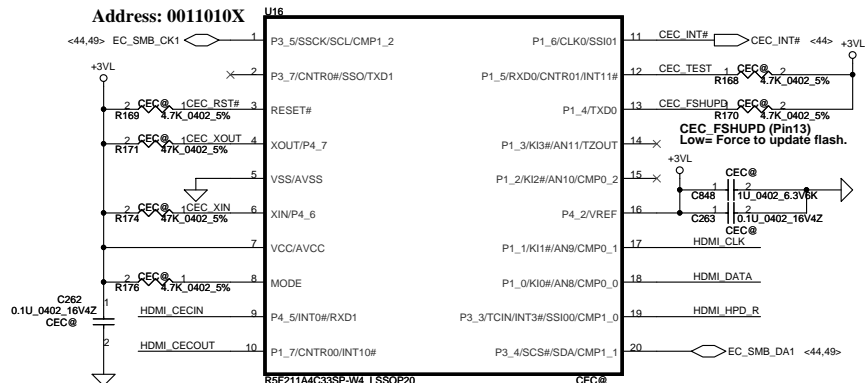
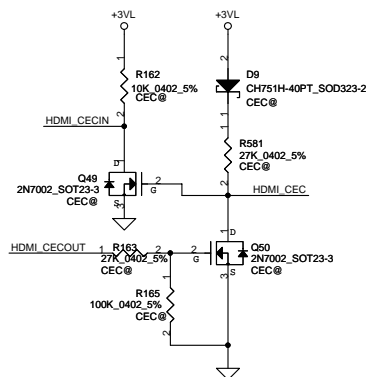


## CRT CONNECTOR



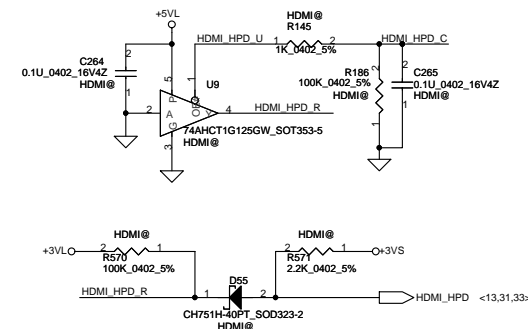
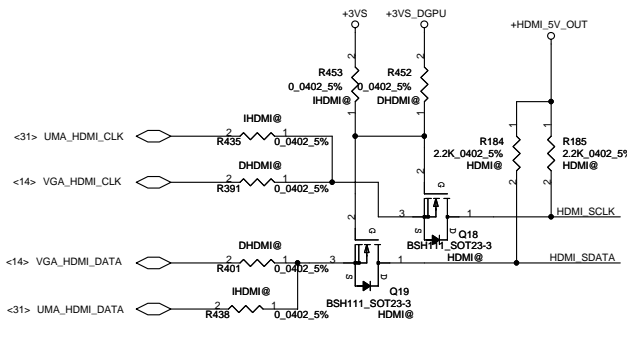
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	40198D
				Date	Monday, February 28, 2011
				Sheet	26 of 59

## HDMI CEC Controller



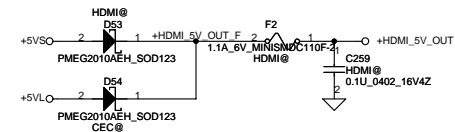
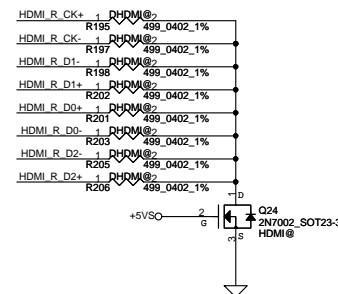
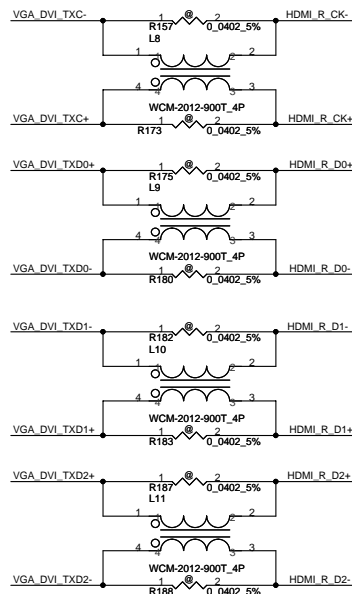
## For DISCRETE

<14>	VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXC+
<14>	VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXC-
<14>	VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXD0+
<14>	VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXD0-
<14>	VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXD1+
<14>	VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXD1-
<14>	VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXD2+
<14>	VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K_DHDM@	VGA_DVI_TXD2-

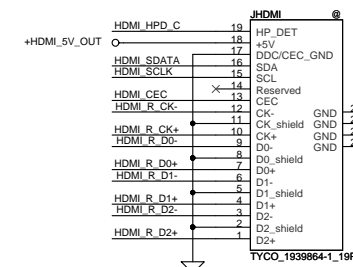


For Optimus

<1>	UMA_HDMI_TXC+	CV308	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXC+
<1>	UMA_HDMI_TXC-	CV304	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXC-
<1>	UMA_HDMI_TX0+	CV306	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXD0
<1>	UMA_HDMI_TX0-	CV302	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXD0-
<1>	UMA_HDMI_TX1+	CV303	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXD1+
<1>	UMA_HDMI_TX1-	CV301	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXD1-
<1>	UMA_HDMI_TX2+	CV307	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXD2+
<1>	UMA_HDMI_TX2-	CV305	1	2	0.1U_0402_16V7K	IHDMI@	VGA DVI_TXD2-

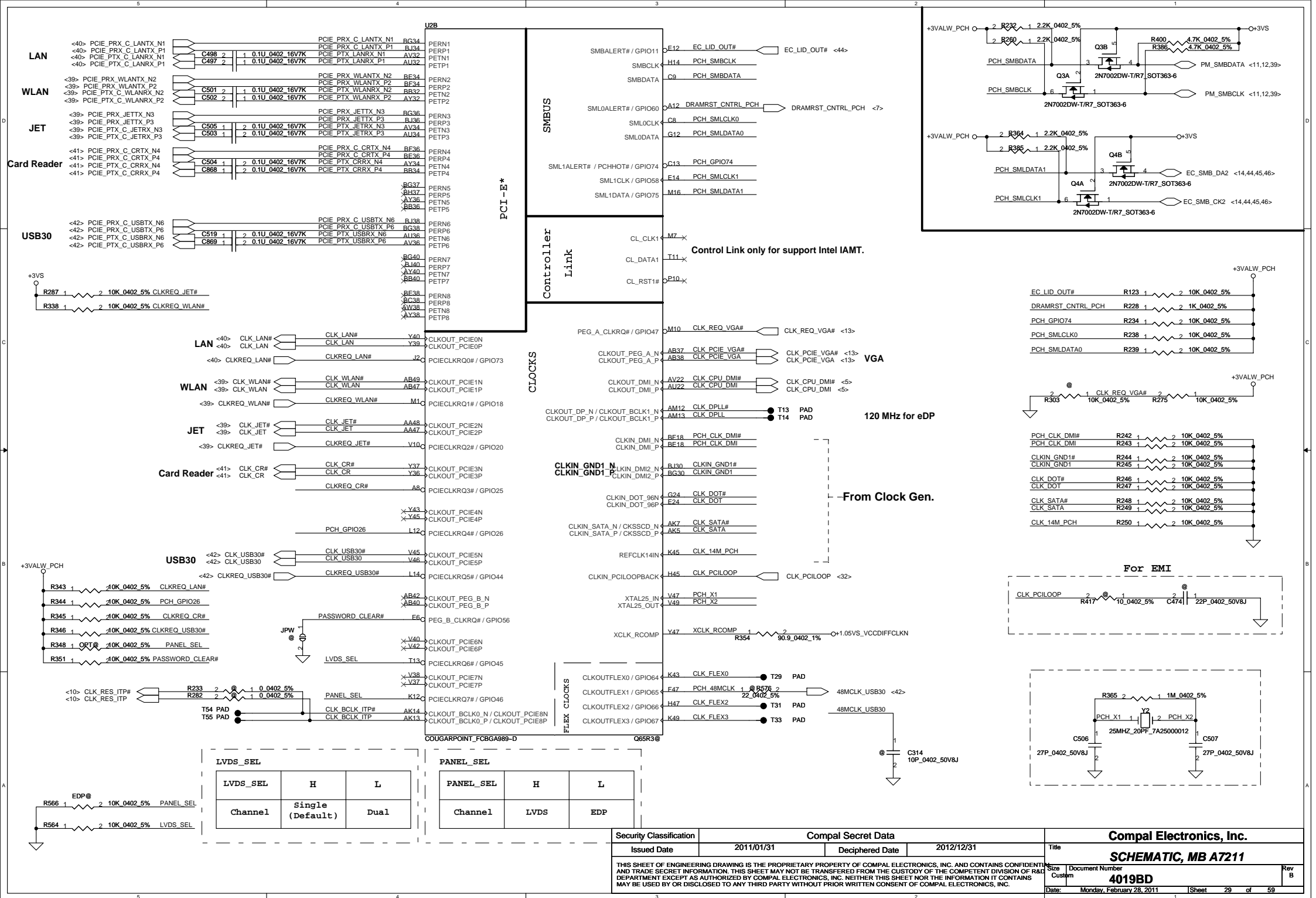


## HDMI Connector

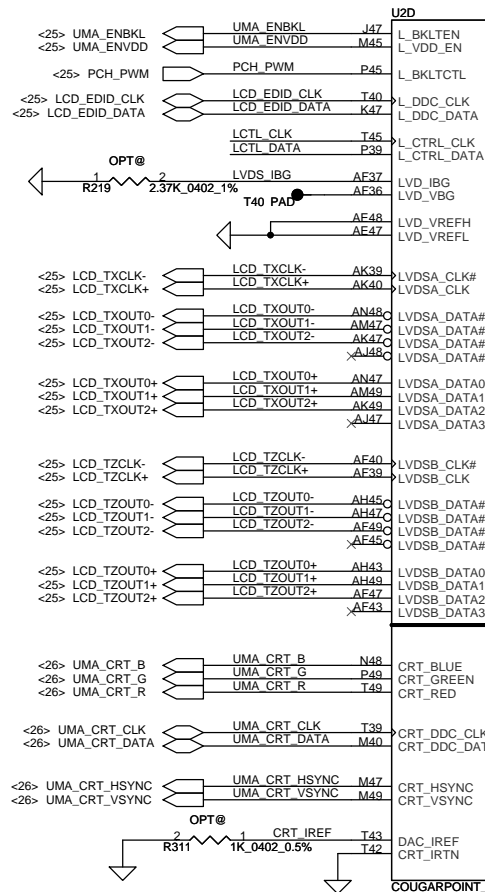
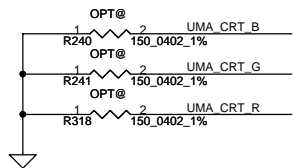
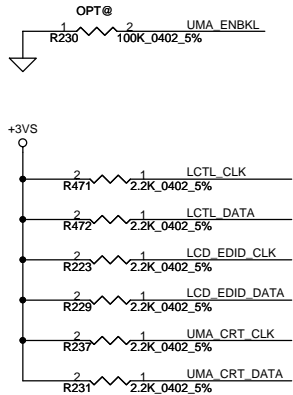


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SCHEMATIC, MB A7211		
				Size	Document Number	Rev B
				4019BD		
Date: Monday, February 28, 2011				Sheet	27	of 59

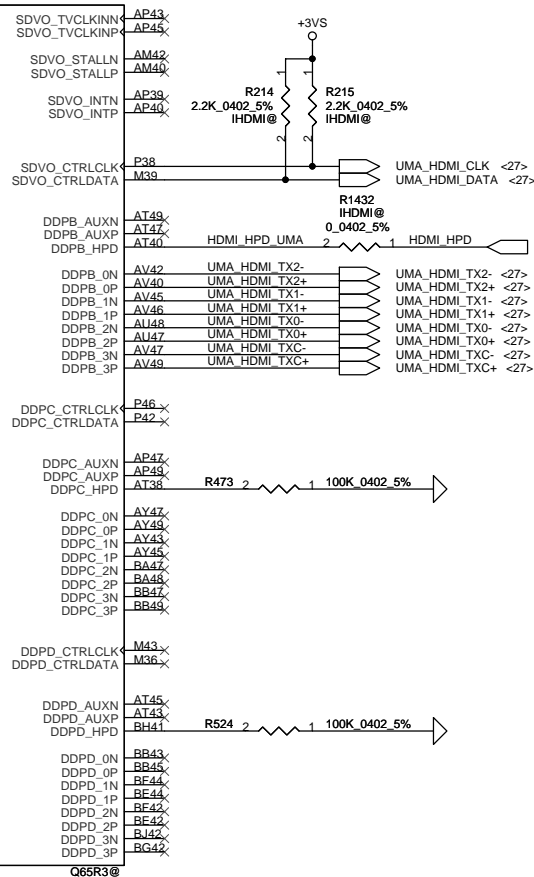






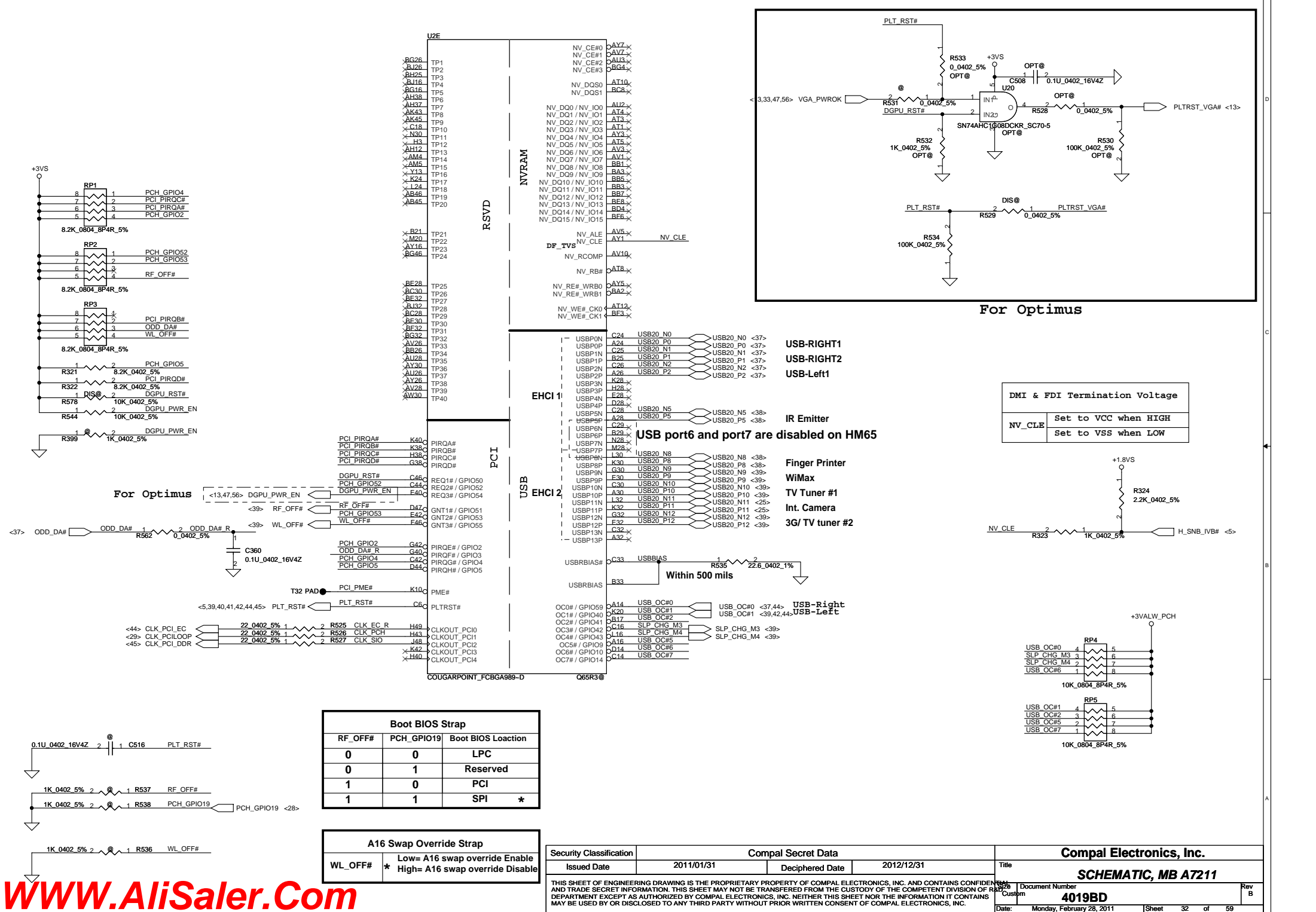


# Digital Display Interface

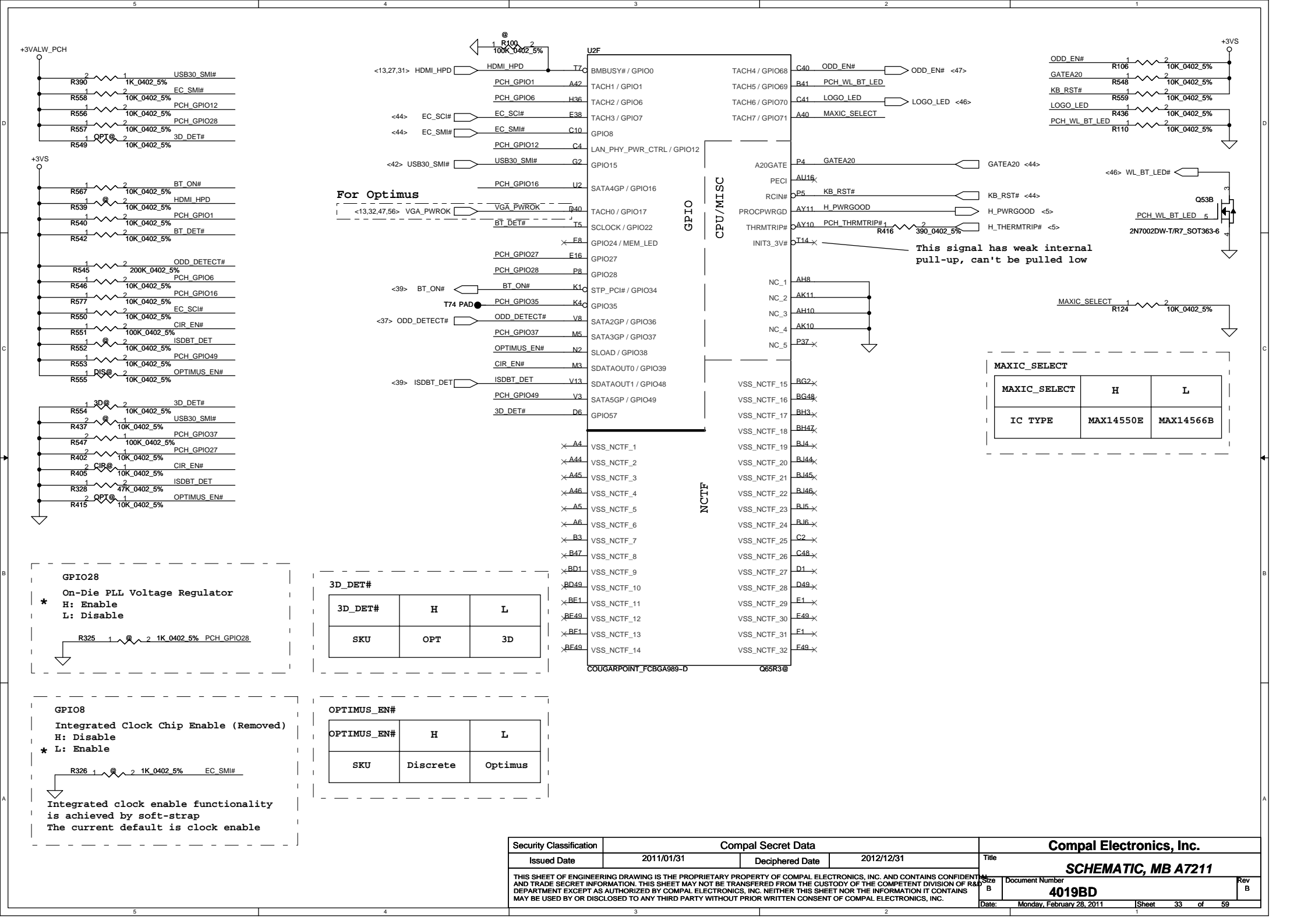


# HDMI

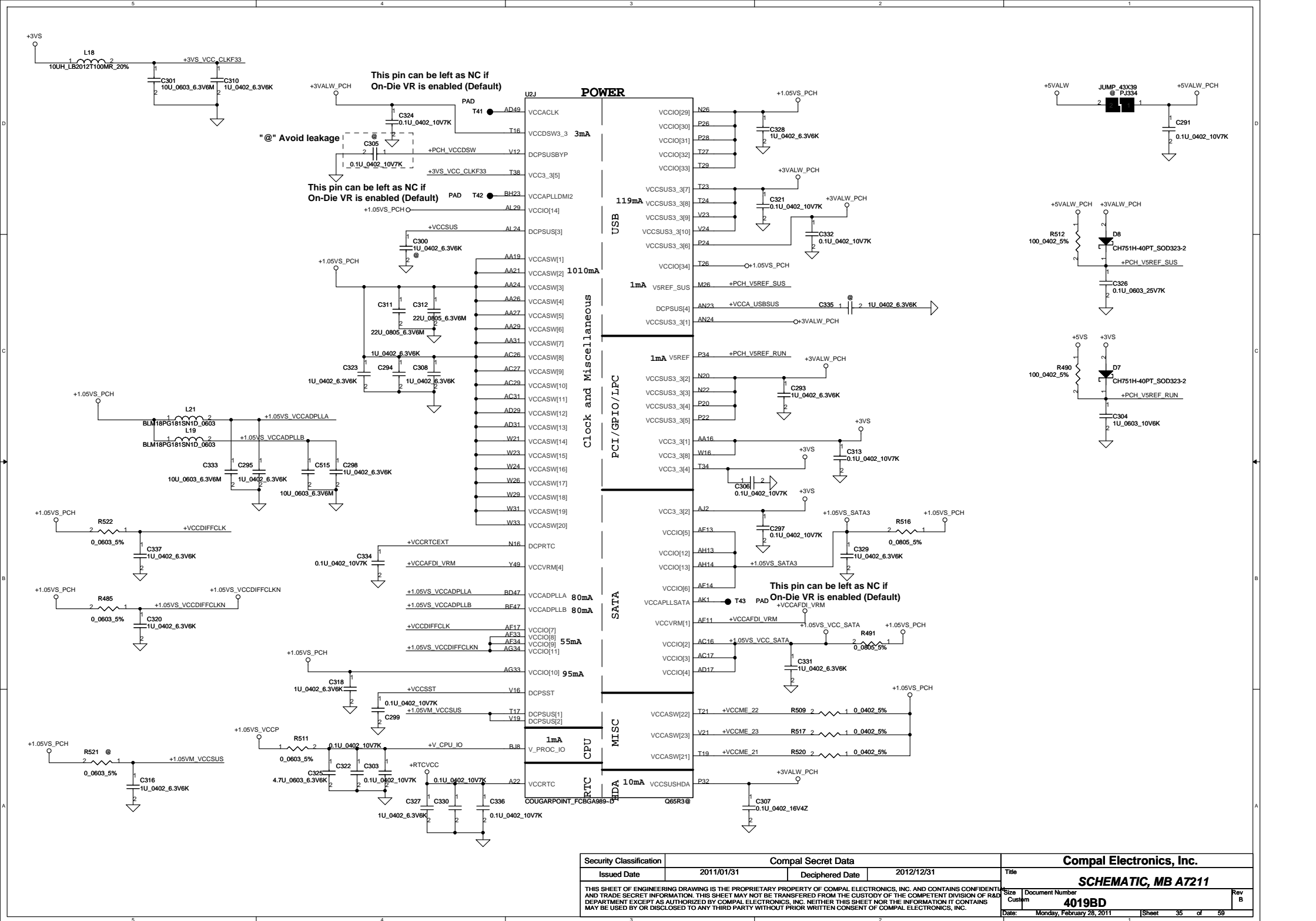
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	40198D
				Date	Monday, February 28, 2011
				Sheet	31 of 59

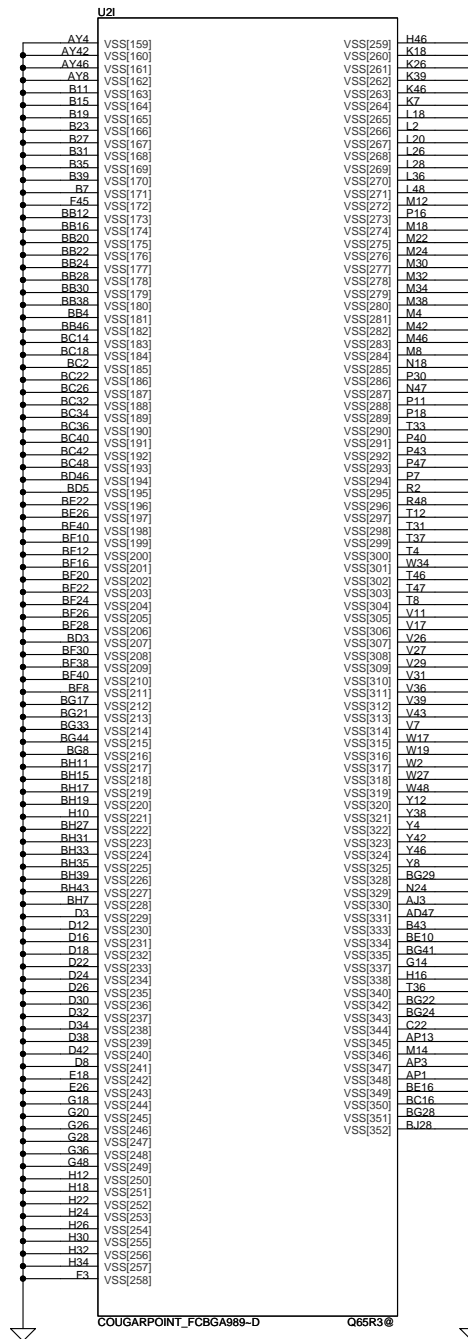
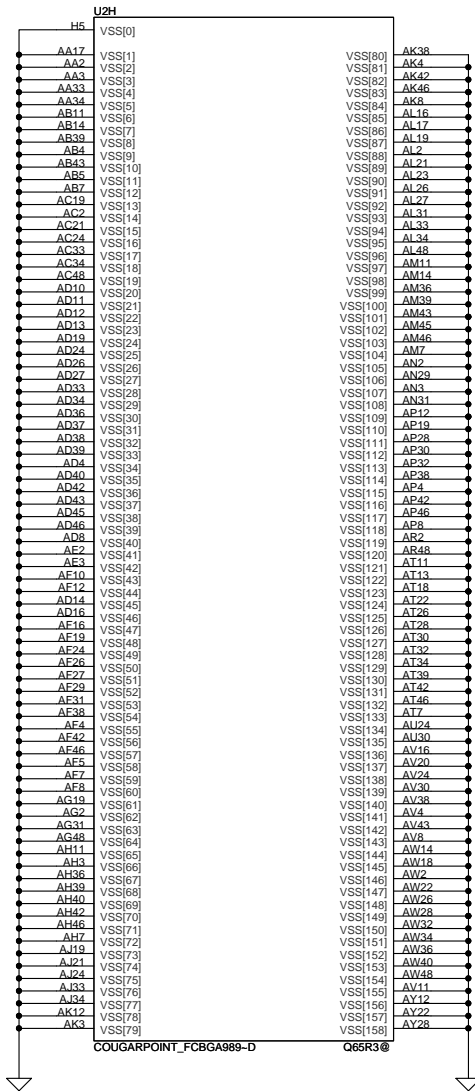






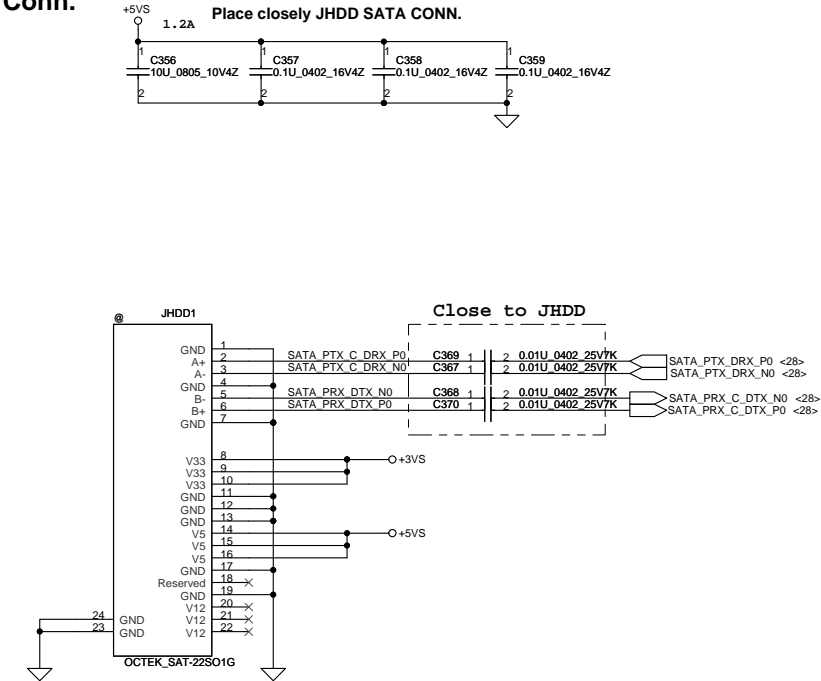




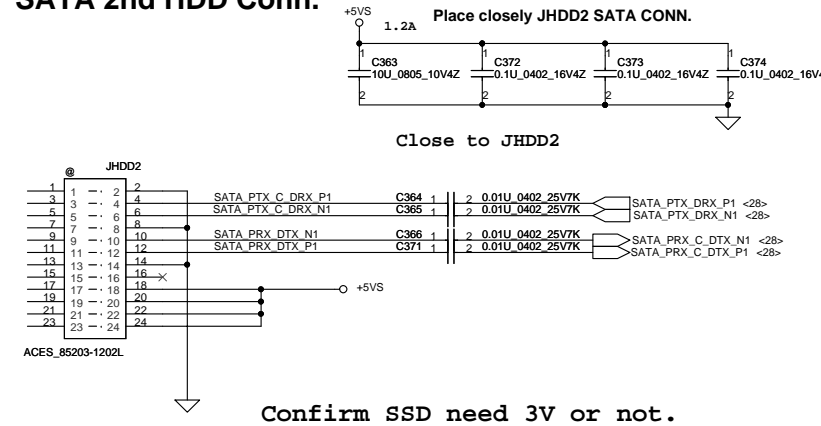


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SCHEMATIC, MB A7211
Document Number				Rev B
4019BD				
Date: Monday, February 28, 2011				Sheet 36 of 59

SATA HDD Conn.

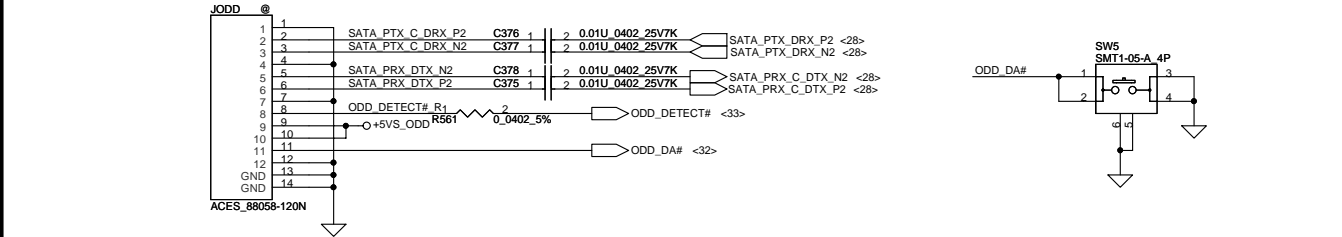


SATA 2nd HDD Conn.

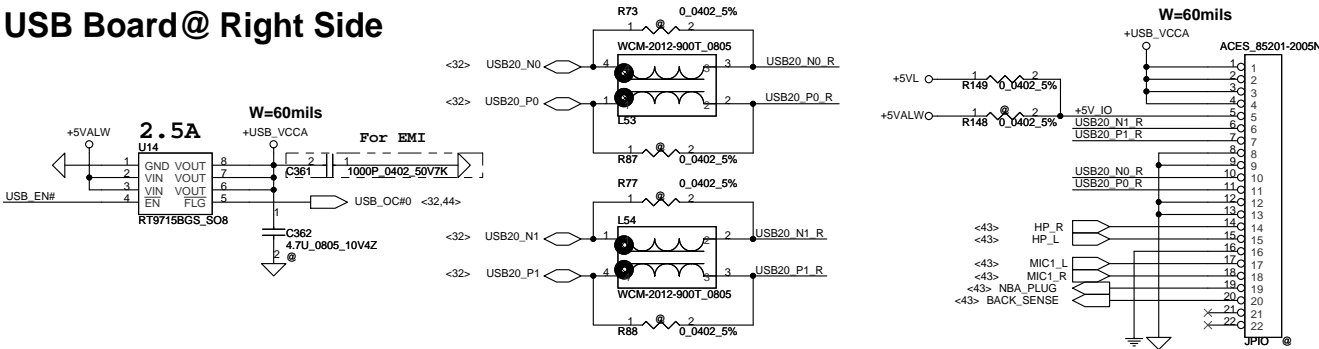


Confirm SSD need 3V or not.

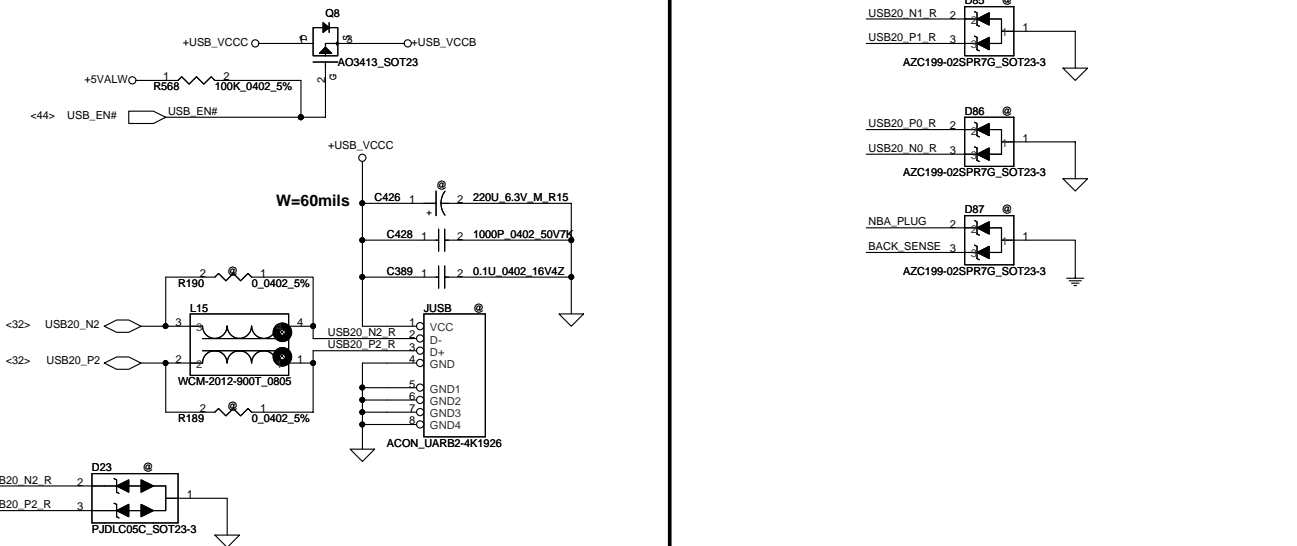
SATA ODD Conn



USB Board@ Right Side

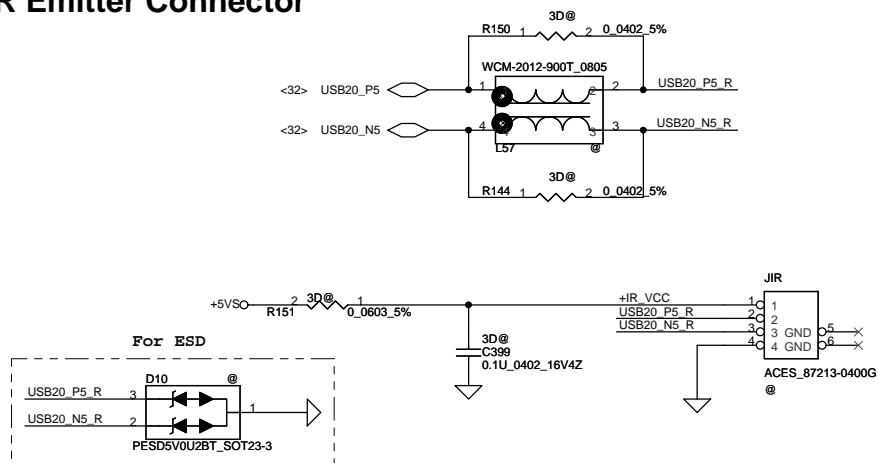


USB Board@ Left Side

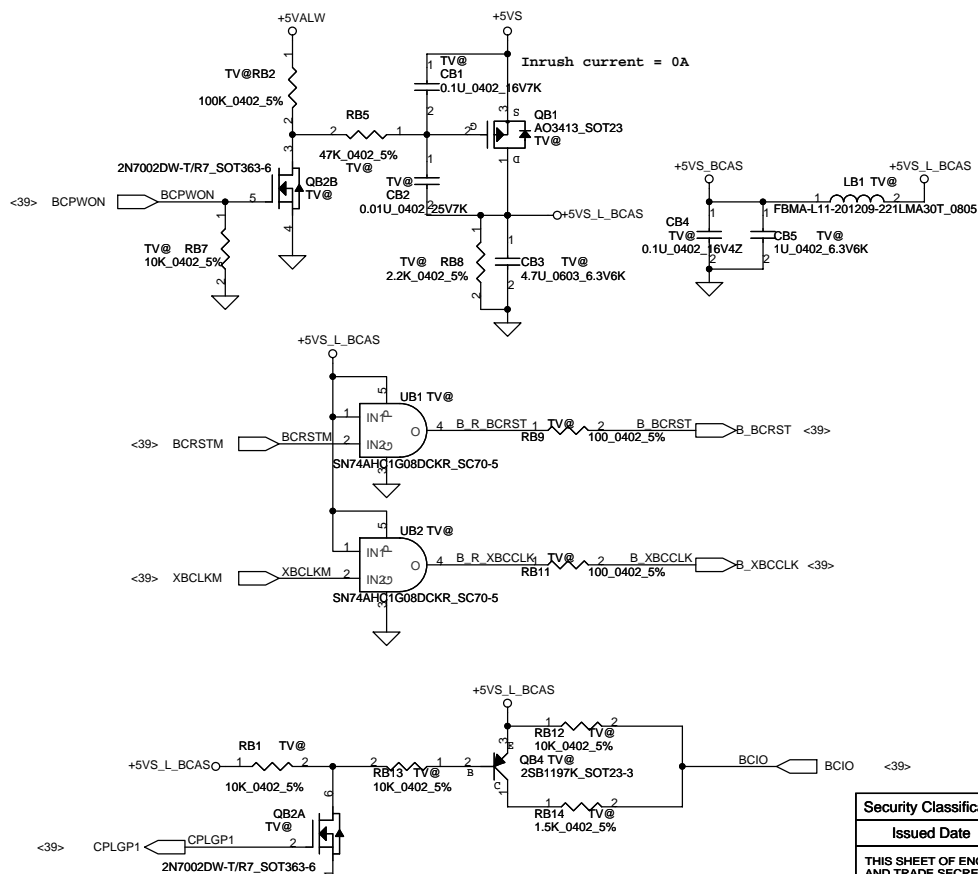


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					4019BD
				Date:	Monday, February 28, 2011
				Sheet	37 of 59

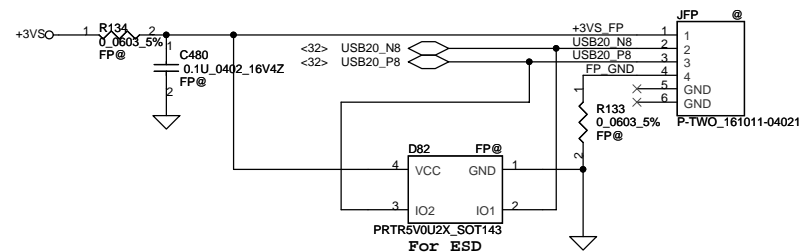
## IR Emitter Connector



## B-CAS Circuit

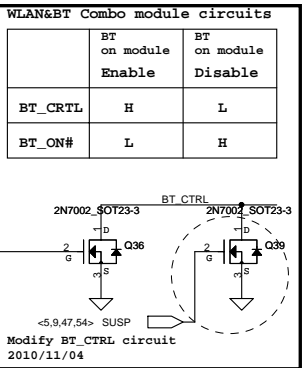
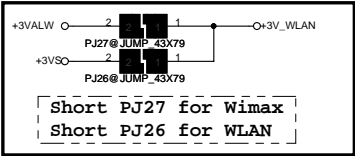


## Finger printer

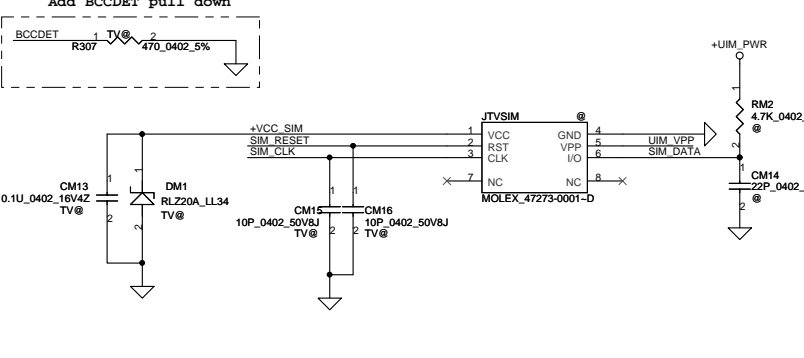
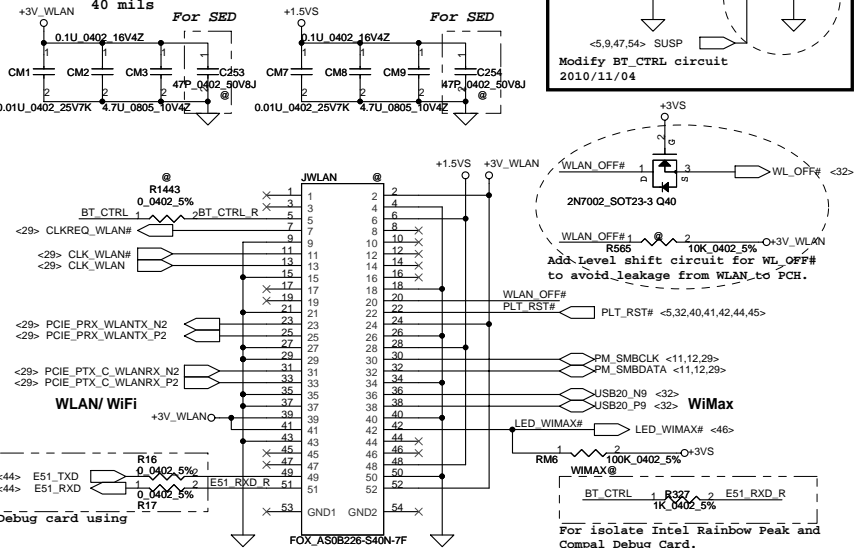
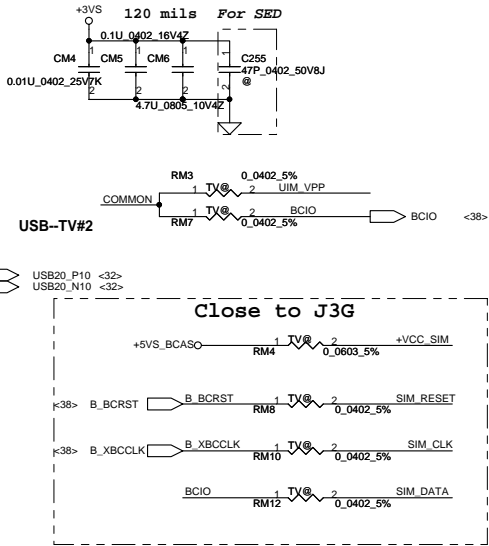
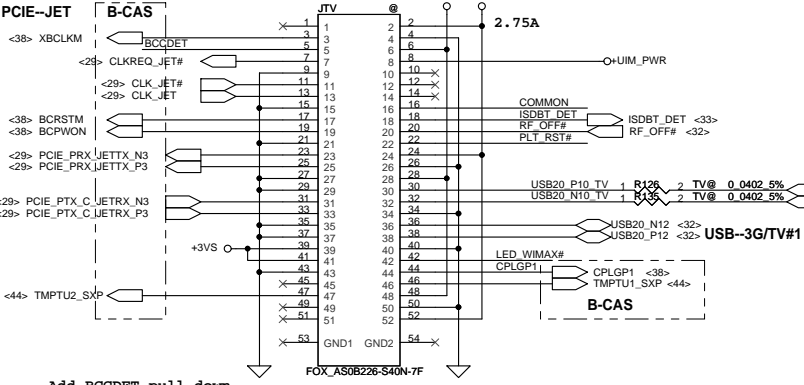


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	38 of 59

Slot 1 Half PCIe Mini Card-WLAN/ WiMax



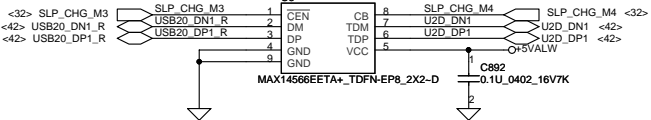
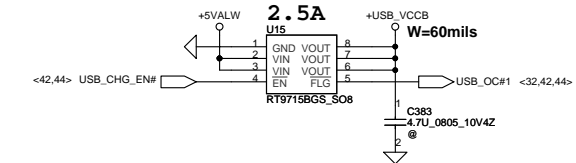
Slot 2 Full PCIe Mini Card- 3G/ TV Tuner  
Half PCIe Mini Card- JET



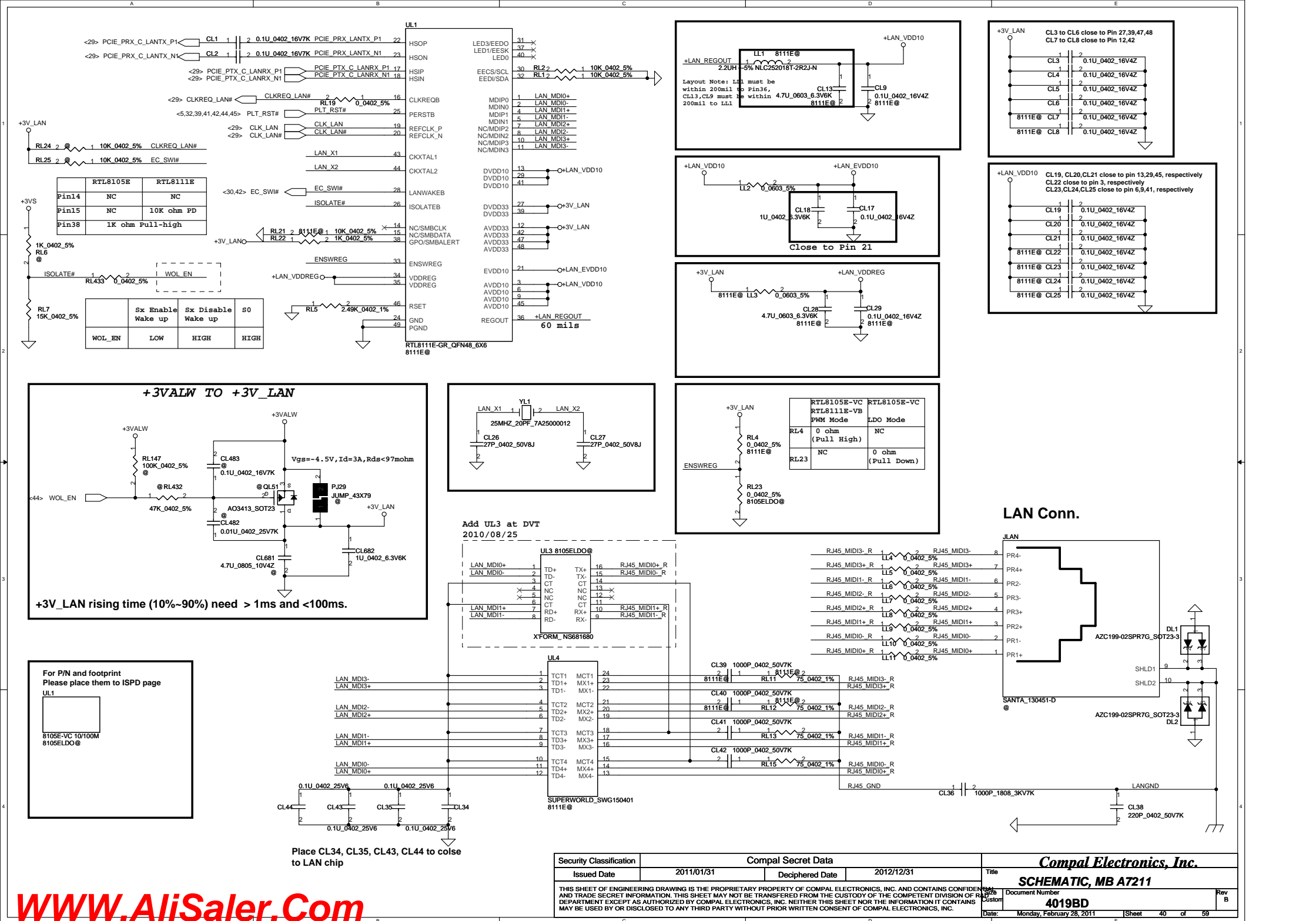
USB Sleep & Charge  
Auto-Mode  
Mode3/Mode4

MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E	
CB0: SLP_CHG_M4	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM



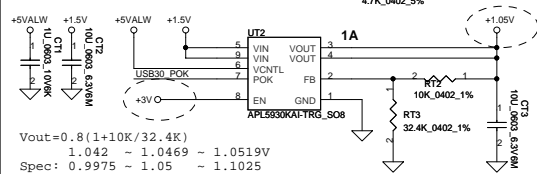
Security Classification		Compal Secret Data		Title	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				4019BD	B
				Date: Monday, February 28, 2011	Sheet 39 of 59



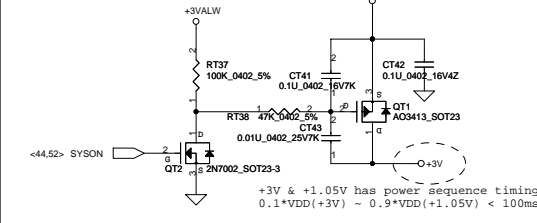




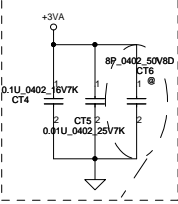
## +1.5V to +1.05V Transfer



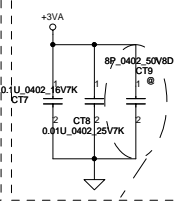
## +3VALW to +3V Transfer



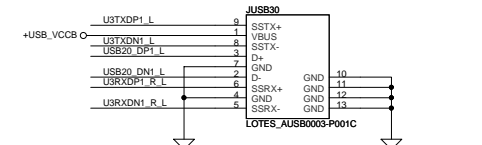
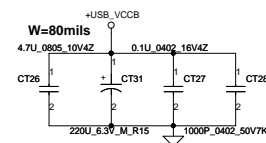
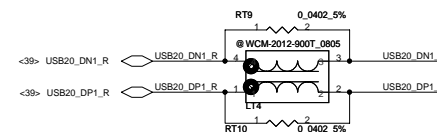
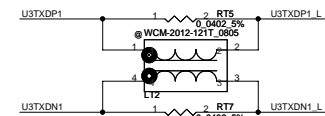
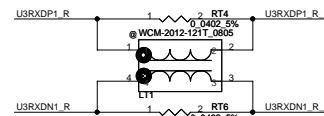
### Close to U102.D7



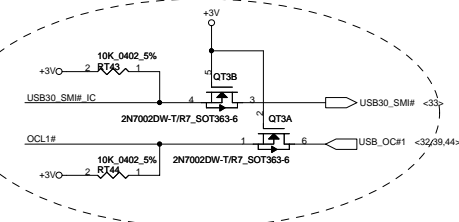
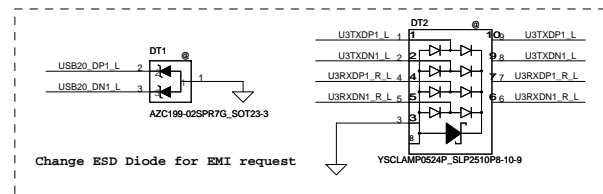
### Close to U102.P13



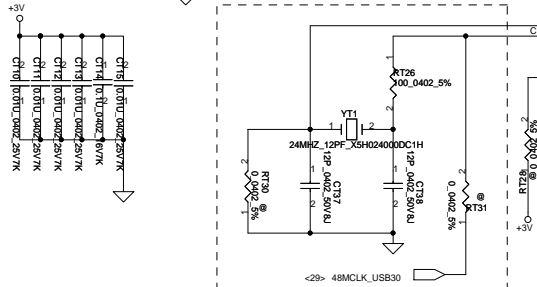
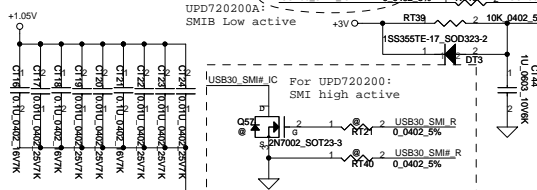
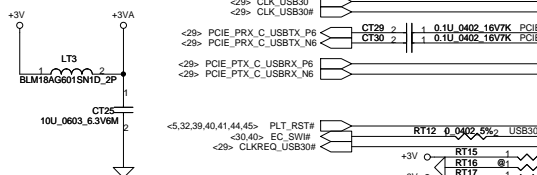
Follow Vendor recommend.



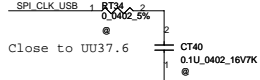
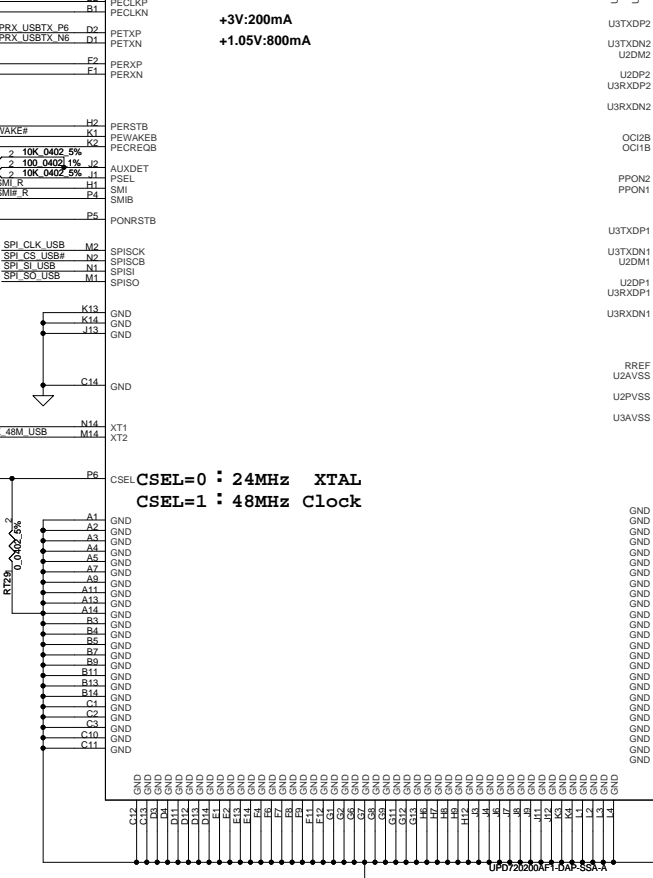
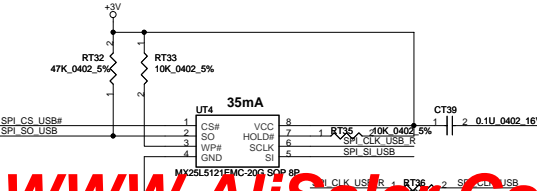
USB30PWIRON RT11 1 2 USB\_CHG\_EN# <39,44>  
0.0402 5%



2010/09/17 Add Level shift to avoid +3V leakage from +3VALW\_PCH



Place as close as possible to  
UU102.N14 and UU102.M14

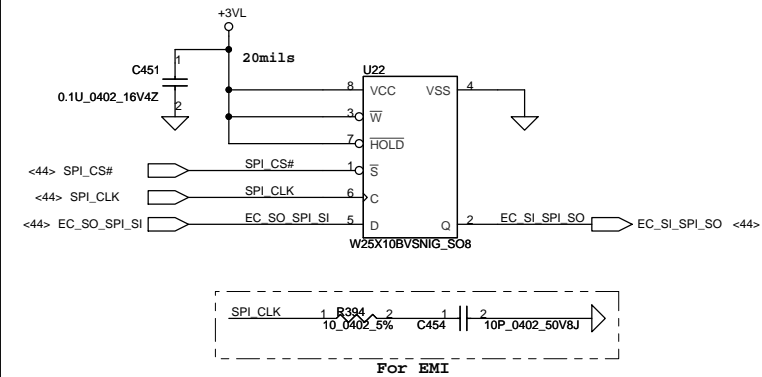


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	SCHEMATIC, MB A7211	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size Custom		Document Number 4019BD	Rev B
Date: Monday, February 28, 2011		Sheet 42 of 59			

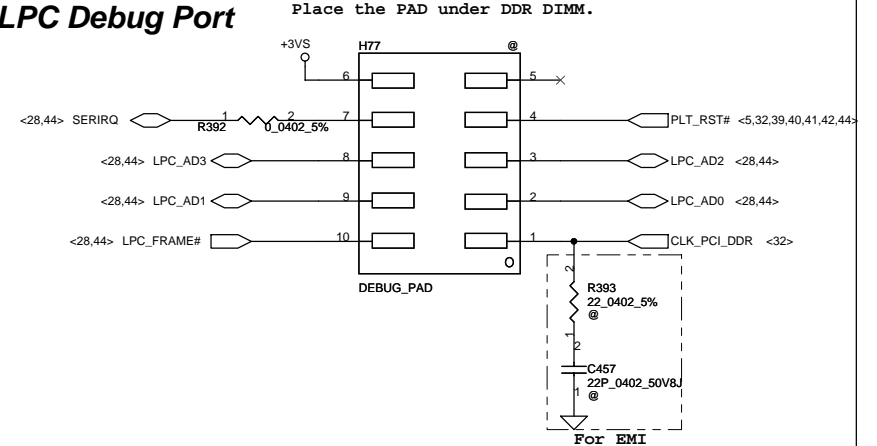




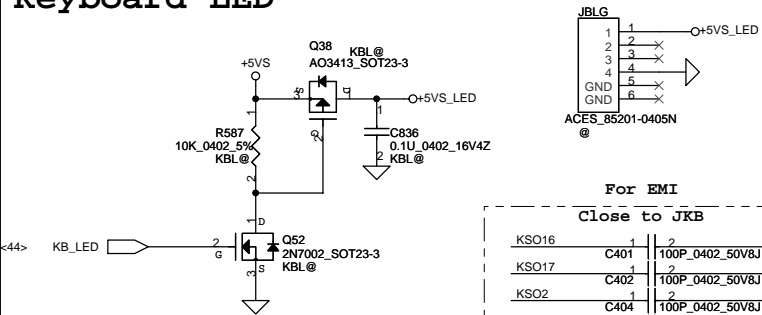
## SPI Flash (256KB)



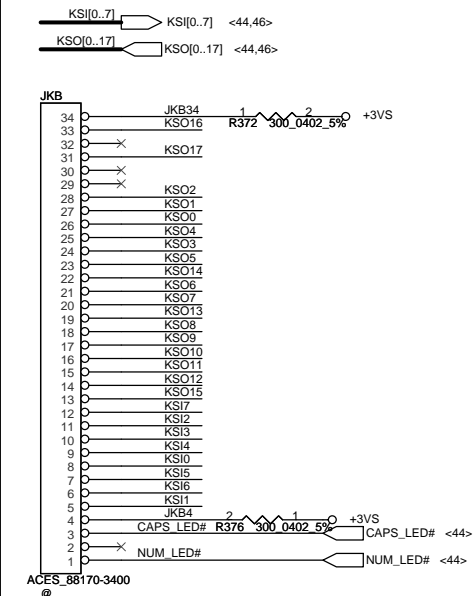
## LPC Debug Port



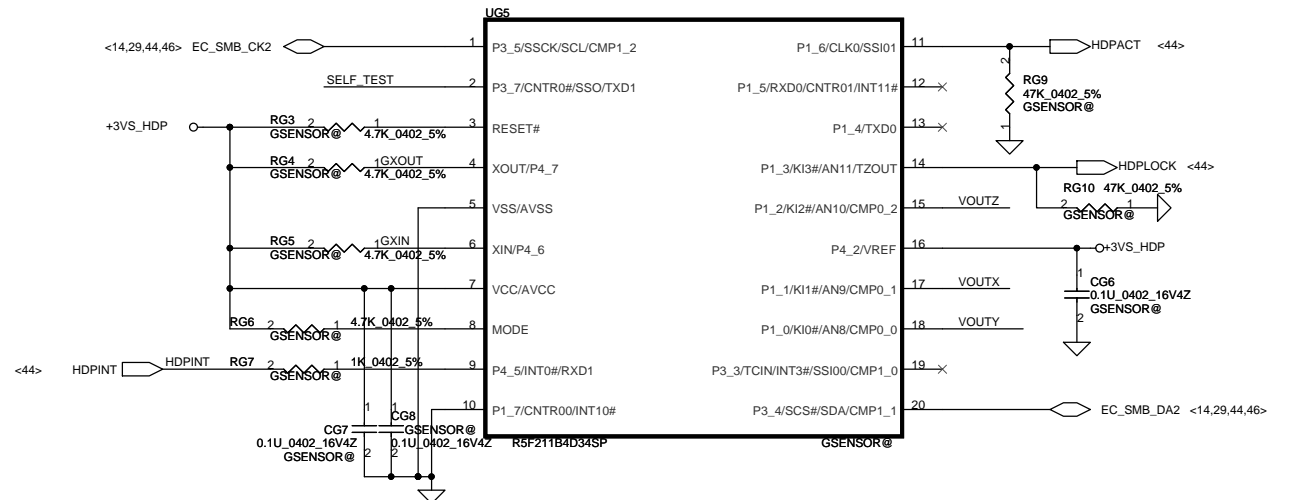
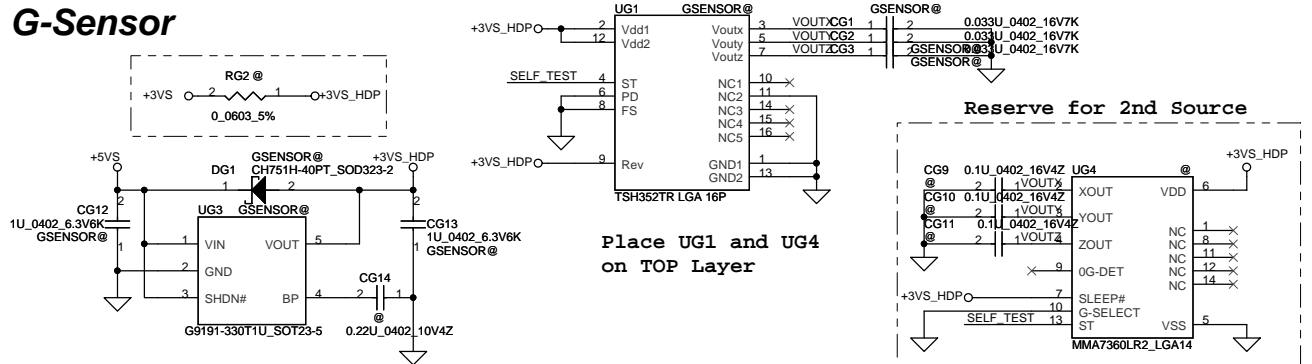
## Keyboard LED



## KEYBOARD CONN.



## G-Sensor



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Document Number
				40198D
				Rev B
				Date: Monday, February 28, 2011
				Sheet 45 of 59



**+3VALW TO +3VS**

$V_{gs}=10V, I_d=9A, R_{ds}=18.5m\Omega$

3VALW

Q29

4.7uF 10V4Z

C465

1uF 0.005 10V4Z

C460

1uF 0.005 10V4Z

C459

1uF 0.005 10V4Z

C466

330K 0.0402\_5%

R412

47K 0.0402\_5%

R409

470.0005\_5%

R406

Q10A

Q10B

SUSP

2N7002DW-T/R7\_SOT363-6

2N7002DW-T/R7\_SOT363-6

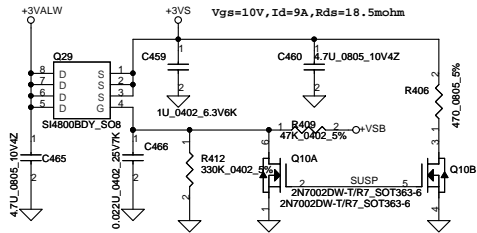
SI4800BDY\_S08

0.02uF 0.0402\_25V7K

3+VALW

3VS

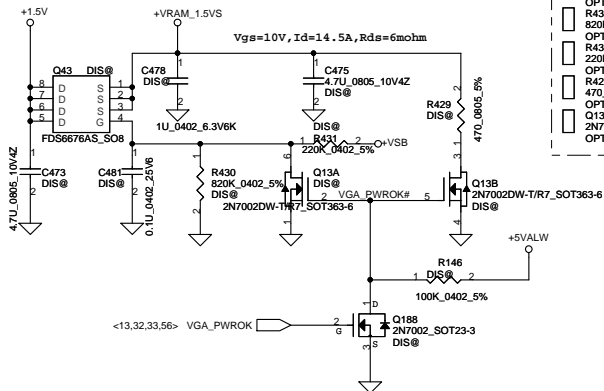
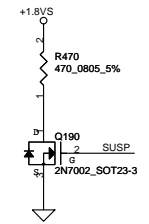
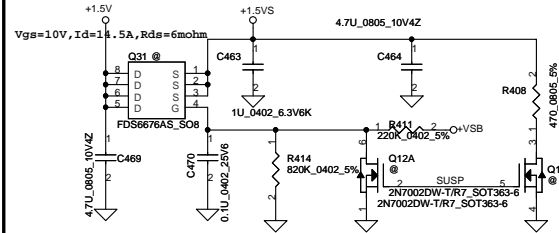
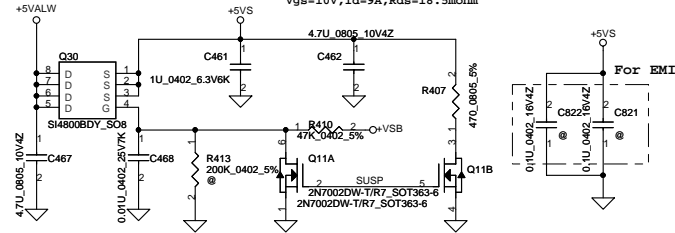
CH+VSB



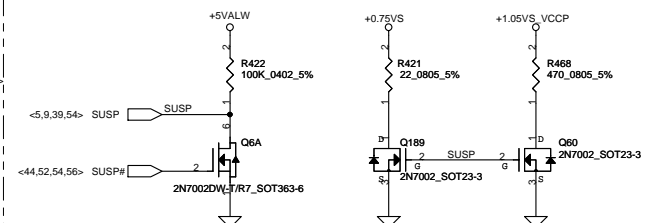
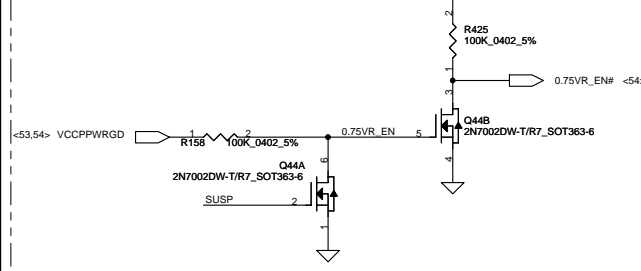
**+5VALW TO +5VS**

Vgs=10V, Id=9A, Rds=18.5mohm

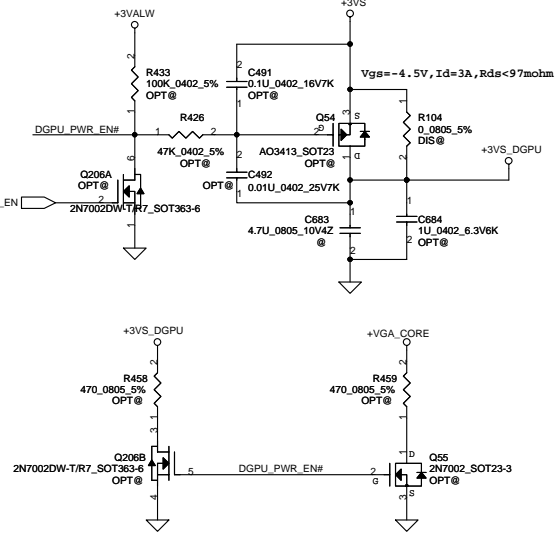
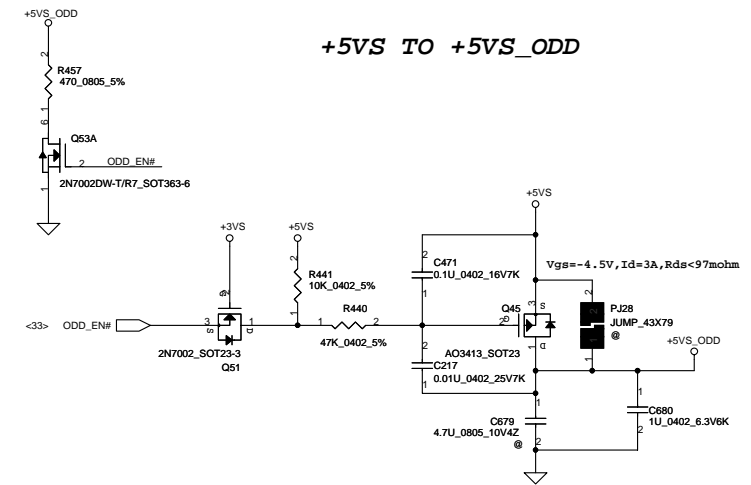
The circuit diagram shows a power MOSFET switching regulator. The input is labeled +5VALW. A diode Q30 (SI4800BDY\_S08) is connected in series with the input. A capacitor C467 (4.7U\_0B05\_10V4Z) is connected across the input. The MOSFET's gate is driven by a +5VS source through a network of capacitors (C461, C462) and resistors (R413, R410). The MOSFET's drain is connected to the output +5VS through a resistor R407 (470\_0B05\_5%). The MOSFET's source is connected to ground through a resistor R413 (200K\_0402\_5%) and a capacitor C468 (0.01U\_0402\_25V7K). The MOSFET is a Si4800BDY\_S08.



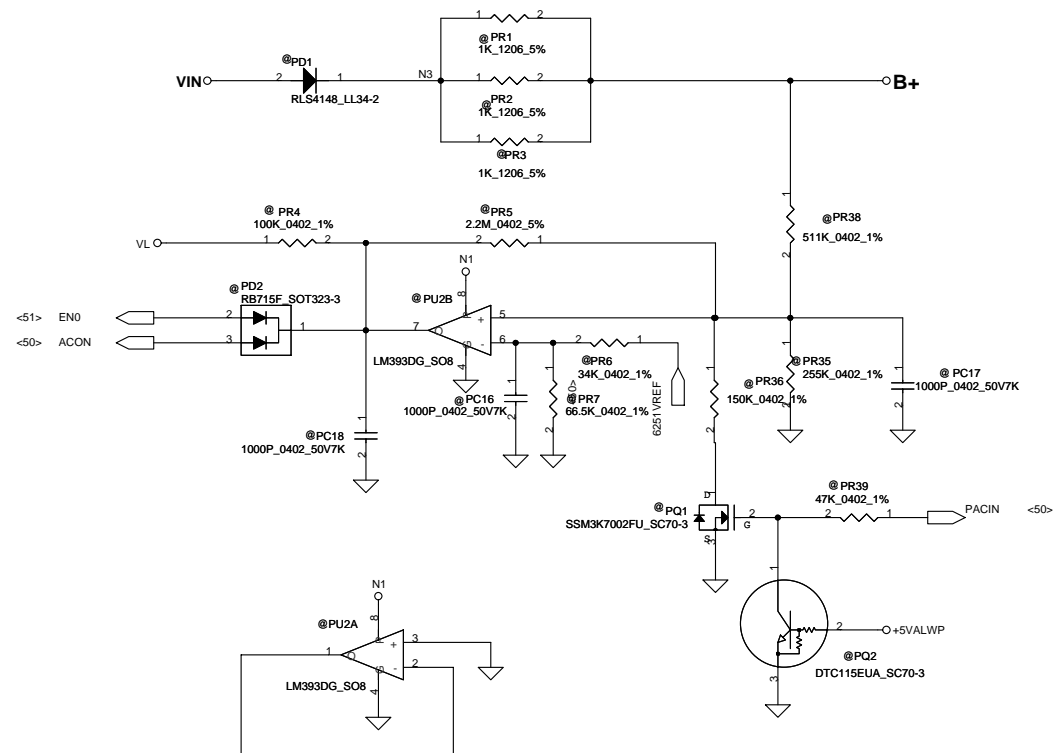
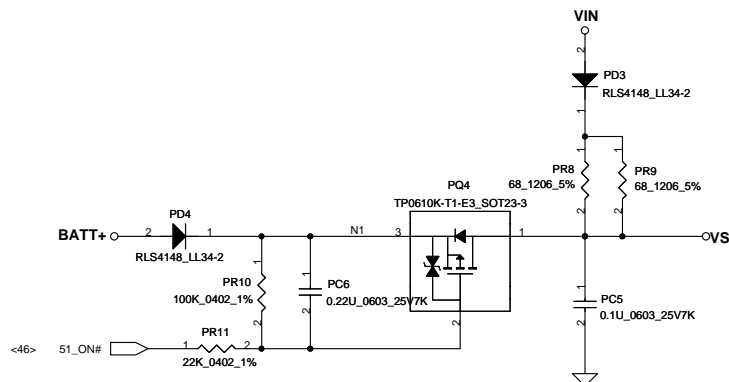
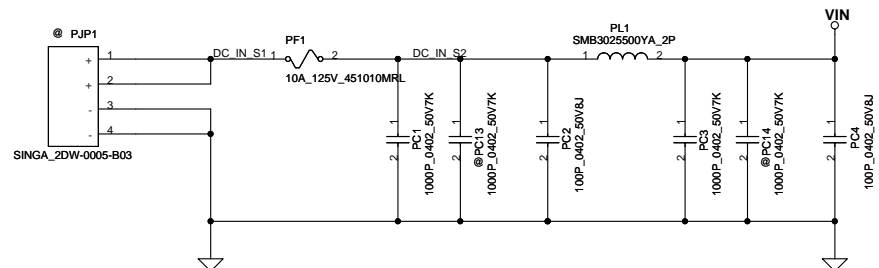
- |  |  |
|--|--|
| <input type="checkbox"/> Q43                   | <input type="checkbox"/> C473            |
| <input type="checkbox"/> FD56676AS_S08         | <input type="checkbox"/> 4.7U_0805_10V4Z |
| <input type="checkbox"/> OPT@                  | <input type="checkbox"/> OPT@            |
| <input type="checkbox"/> C481                  | <input type="checkbox"/> C478            |
| <input type="checkbox"/> 0.1U_0402_25V6        | <input type="checkbox"/> 1U_0402_6.3V6K  |
| <input type="checkbox"/> R430                  | <input type="checkbox"/> OPT@            |
| <input type="checkbox"/> 820K_0402_5%          | <input type="checkbox"/> C475            |
| <input type="checkbox"/> OPT@                  | <input type="checkbox"/> 4.7U_0805_10V4Z |
| <input type="checkbox"/> R431                  | <input type="checkbox"/> OPT@            |
| <input type="checkbox"/> 220K_0402_5%          | <input type="checkbox"/> R146            |
| <input type="checkbox"/> OPT@                  | <input type="checkbox"/> 100K_0402_5%    |
| <input type="checkbox"/> R429                  | <input type="checkbox"/> OPT@            |
| <input type="checkbox"/> 47U_0805_5%           | <input type="checkbox"/> Q188            |
| <input type="checkbox"/> OPT@                  | <input type="checkbox"/> 2N7002_SOT23-3  |
| <input type="checkbox"/> Q13                   | <input type="checkbox"/> OPT@            |
| <input type="checkbox"/> 2N7002DW-T/R_SOT363-6 |  |
| <input type="checkbox"/> OPT@                  |  |

[illegible]

The schematic shows two MOSFET drivers connected to the DGPU\_PWR\_EN# signal. The top driver uses a 2N7002DW-T/R7 MOSFET (Q206A) driven by Q206A OPT#. It has a pull-up resistor R433 (100K\_0402\_5% OPT#) from +3VALW and a source resistor R426 (47K\_0402\_5% OPT#). The bottom driver uses a 2N7002DW-T/R7 MOSFET (Q206B) driven by Q206B OPT#. It also has a pull-up resistor R458 (470\_0805\_5% OPT#) from +3VS\_DGPU. Both drivers output to the DGPU\_PWR\_EN# node, which is connected to the gate of the main power MOSFET Q54 (AO3413\_SOT23 OPT#). Q54's drain is connected to +3VS through a resistor network (R104, C491, C492, C683, C684) and its source is connected to ground through a diode (D5).

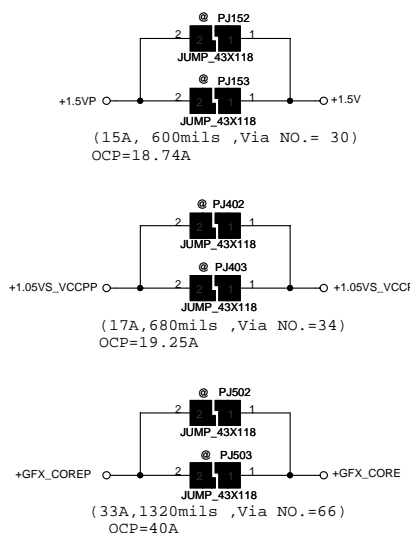
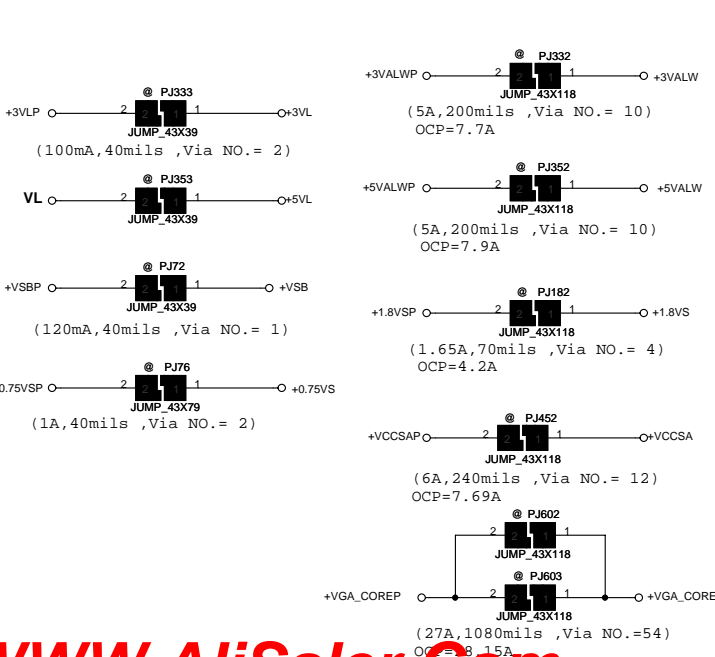
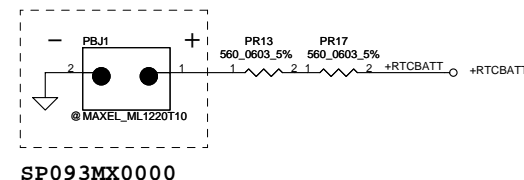
[illegible]

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	<b>SCHEMATIC, MB A7211</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	Rev B
				Document Number	
				4019BD	
Date:	Monday, February 28, 2011	Sheet	47	of	59



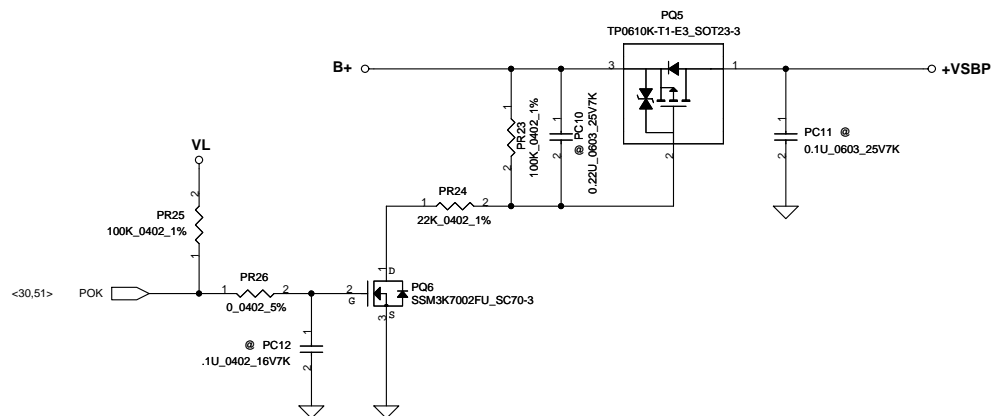
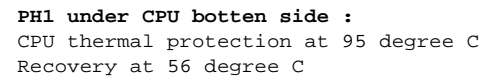
ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

### RTC Battery



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/01/31				Title			
Deciphered Date				2012/12/31				SCHEMATIC, MB A7211			
Document Number				4019BD				Rev B			
Date				Monday, February 28, 2011				Sheet 48 of 59			

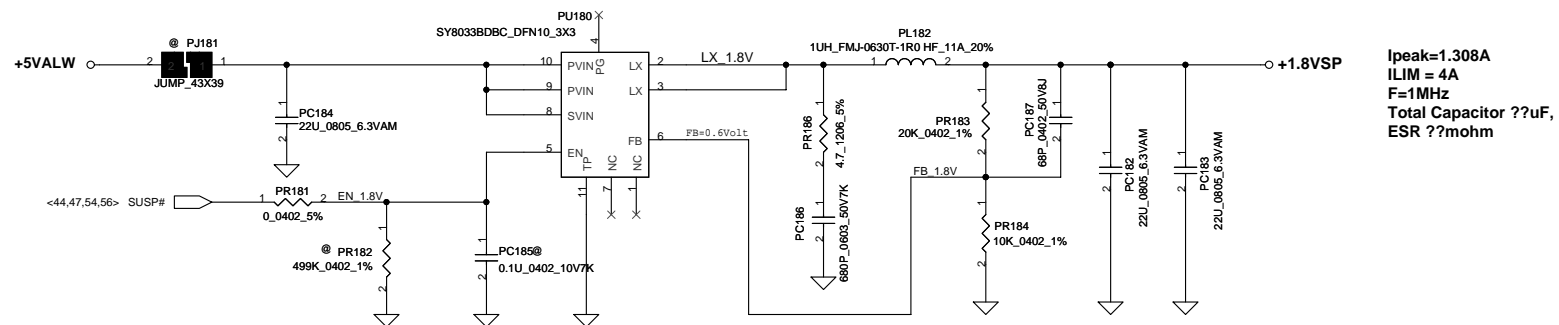
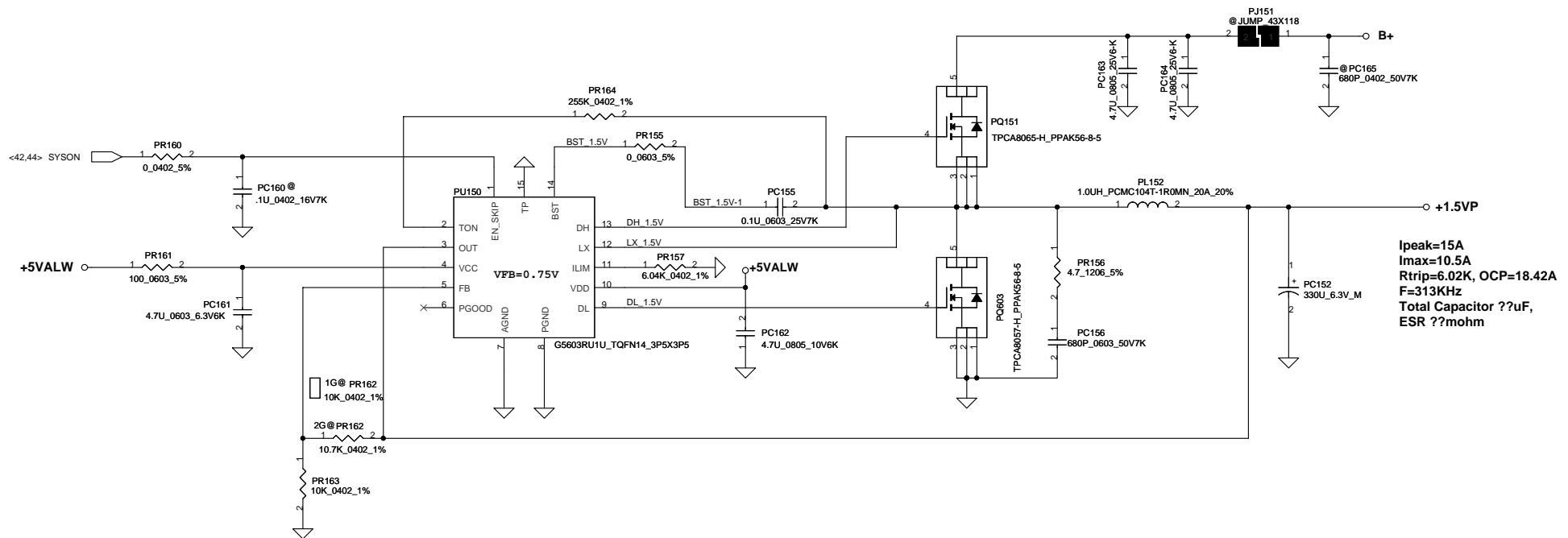




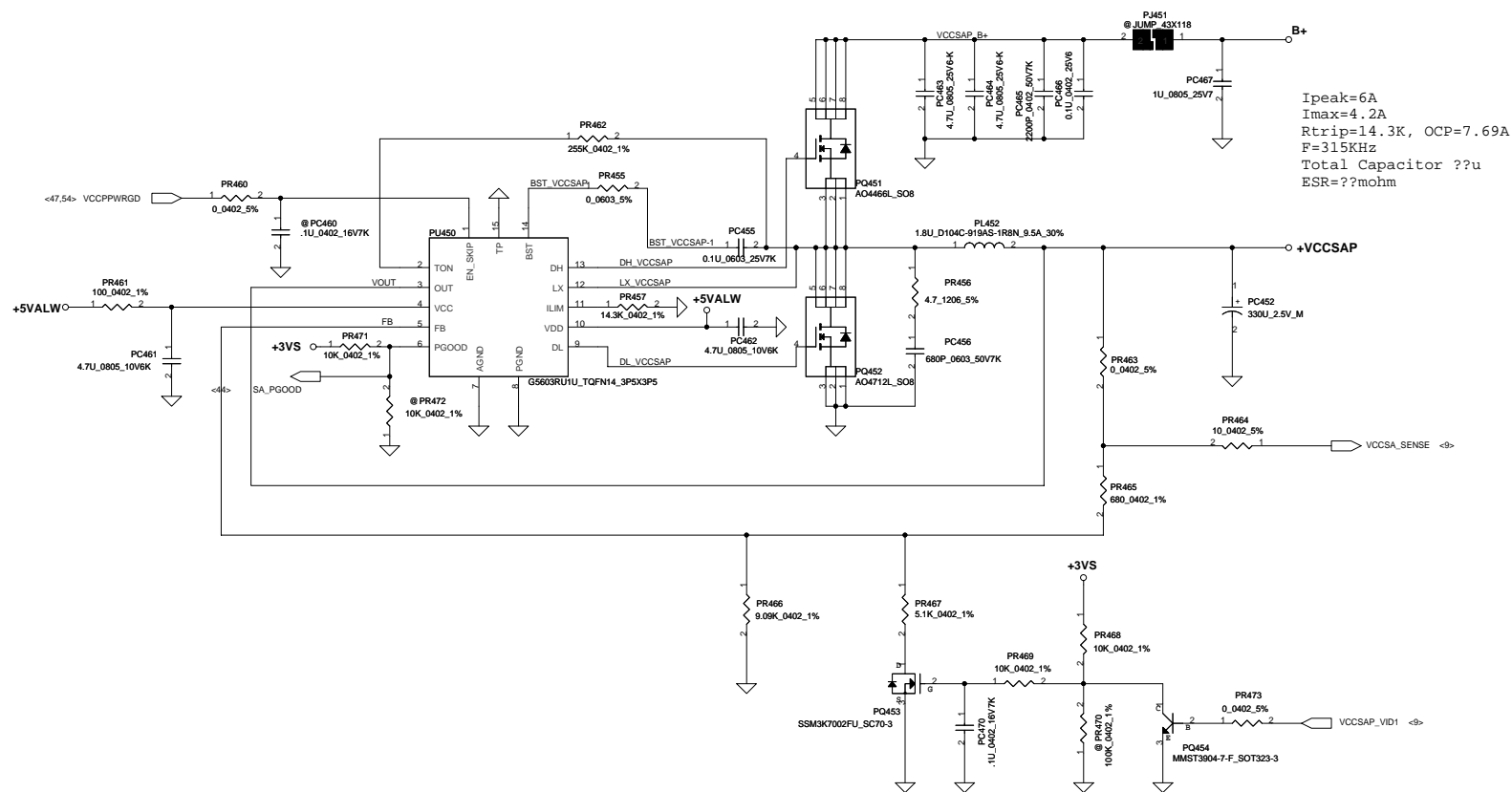
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/01/31		Deciphered Date		2012/12/31		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		SCHEMATIC, MB A7211							
		Doc#		Document Number				Rev B	
		4019BD							
		Date:		Monday, February 28, 2011		Sheet		49 of 59	



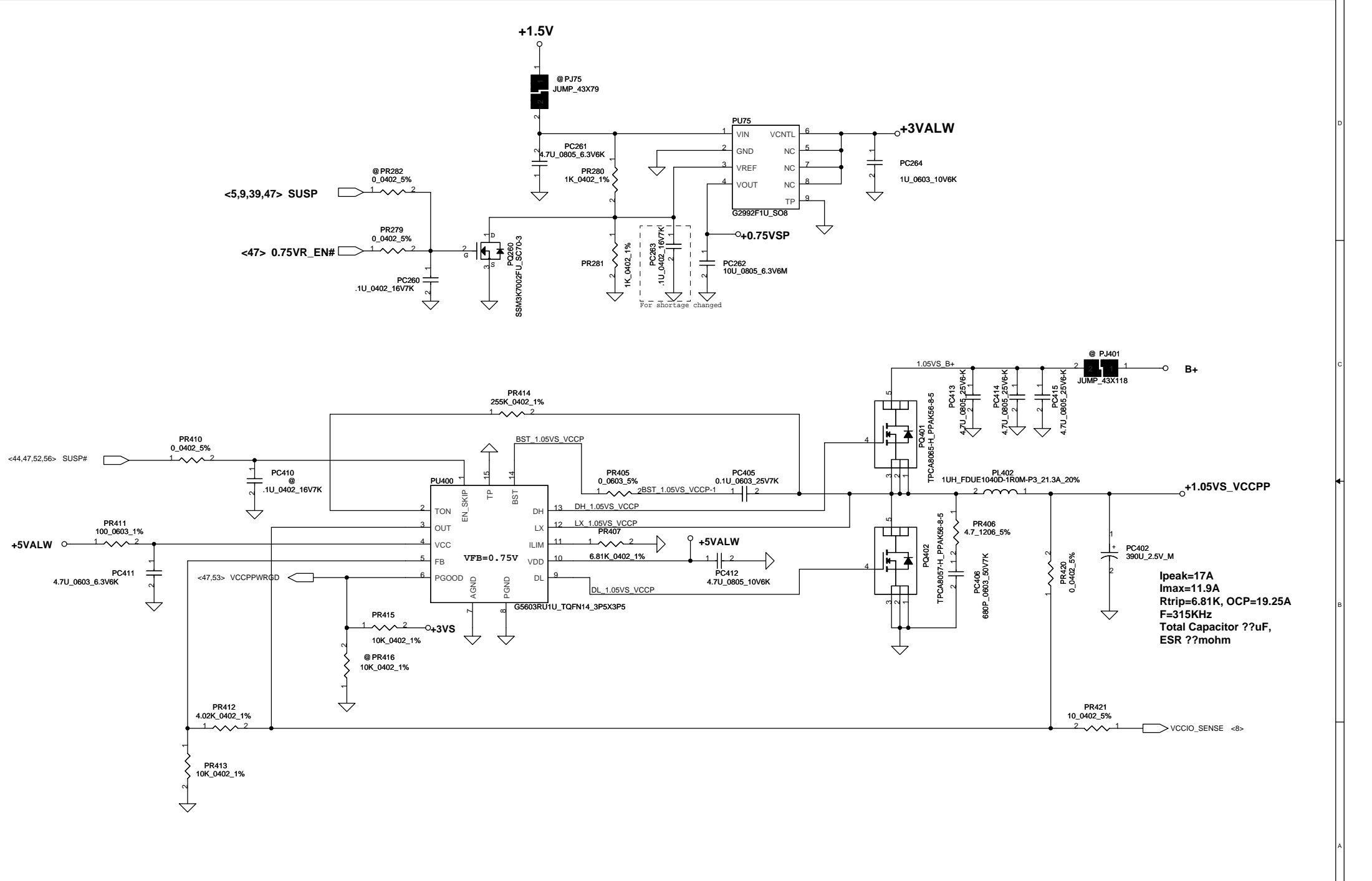




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	<b>SCHEMATIC, MB A7211</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	<b>4019BD</b>
				Date:	Monday, February 28, 2011
				Sheet	52 of 59

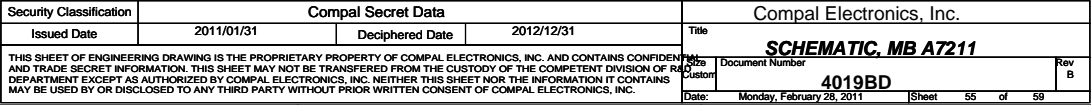


VID1	+VCCSAP
1	0.8V
0	0.9V



Ipeak=17A  
I<sub>max</sub>=11.9A  
R<sub>trip</sub>=6.81K, OCP=19.25A  
F=315KHz  
Total Capacitor ??uF,  
ESR ??mohm

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	54 of 59







NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	
	2010/10/23	P49	Change PR29 to 100K,Delete PQ7	Circuit modify
	2010/10/23	P50	Change PQ204 to AO4409L,PR210 to 200K ohm,PR211 to 47k ohm	Circuit modify
			Change PQ212 to SB00000EO00,delete PQ218 ,add PR206,PC206	
			Change PR222 to 53.6K ohm,PR223 to 20k ohm for L01	
	2010/10/23	P51	Change PQ360 to SB00000EO00	Circuit modify
	2010/10/23	P52	Change PR157 to 6.04K ohm,PQ151 to TPCA8065,PQ603 TPCA8057	Circuit modify
			Change PL152 to 1UH,add PR156,PC156	
	2010/10/23	P53	Change PC452 to 220U_4.3mm height,add PR456,PC456	Circuit modify
	2010/10/23	P54	Change PQ401 to TPCA8065,PQ402 TPCA8057,add PR406,PC406	Circuit modify
	2010/10/23	P55	Add 3rd phase function,PC569,PC574,delete PC568,PC566	Circuit modify
			Change All high side to TPCA8065,all low side to TPCA8057	
			Add GFX function for L01,L03,add all sunnber	
	2010/10/23	P56	Add VGA_CORE function	Circuit modify
	2010/11/29	P48	Disable Pre charge function	Circuit modify
	2010/11/29	P49	Change PR22 to 3.48KΩ,PR28 to 30.9KΩ,PR27,PR31 to 100KΩ	Circuit modify
			PR20 to 17.8KΩ, add PQ7	
	2010/11/29	P50	Change PR219 to 100KΩ,PL201 to 1UH,add PC204,PQ218	Circuit modify
			Change PR222 to 6.34KΩ,PR234 to 3.24KΩ,PR223 to 20KΩ	N12P-GS SKU
			Change PR222 to 53.6KΩ,PR234 to 5.49KΩ,PR223 to 20KΩ	N12P-GV SKU
			Add PC209,PC224	EMI request
	2010/11/29	P51	Add pc225	EMI request
	2010/11/29	P54	Change PR407 to 6.81KΩ	Circuit modify
	2010/11/29	P55	Add pc560	Circuit modify
	2010/11/29	P56	Change PR624 to 95.3KΩ,PR632 to 3.57KΩ,PR640 to 105KΩ	N12P-GS SKU
			PR633 to 16.5KΩ,PR641 to 20KΩ	
			Change PR624 to 71.5KΩ,PR632 to 3.57KΩ,PR640 to 105KΩ	N12P-GV SKU
			PR633,PR641 to 16.5KΩ	
	2010/12/29	P49	Change PR27 to 15.8KΩ,PR28 to 20KΩ,PR30 to 14.7KΩ	N12P-GV SKU
			Change PR27 to 120KΩ,PR28 to 10KΩ,PR30 to 11KΩ	N12P-GS SKU
	2010/12/29	P50	Change PR219 to 100Ω	Circuit modify
			Change PR222 to 10KΩ,PR223 to 33KΩ,PR234 to 10.7KΩ,PR215 to 20mΩ	N12P-GV SKU
			Change PR222 to 8.25KΩ,PR223 to 26.7KΩ,PR234 to 4.12KΩ	N12P-GS SKU
	2010/12/29	P55	Change PC549 to 0.22U_0603_25V	Circuit modify
	2010/12/29	P56	Change PU600 to RT8237C	Circuit modify
			Change PR624 to 118K	OCP modify
	2011/02/09	P49	Change PQ219,PQ220 to SB000009610	Circuit modify
	2011/02/09	P50	Change PC209 to 4.7U_0805,PQ218 to SB000009610	Circuit modify
			Add PR246,PR247,PR248,PC223	Add ADP_V
	2011/02/09	P52	Add PR186,PC186	Circuit modify
	2011/02/09	P53	Change PC452 to 330U_4.2H	Circuit modify
	2011/02/10	P55	Change PC537 to 47P_0403	Circuit modify

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title		
				SCHEMATIC, MB A7211		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					4019BD	B
				Date:	Monday, February 28, 2011	Sheet 57 of 59

# HW PIR (Product Improve Record)

PHRAA LA-7211P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2010/10/26

Item	Date	Page	Component	Solution	Request
------	------	------	-----------	----------	---------

Base LA-6831 0929 schematic to modify

Delete 14550@

Delete 3G@

Delete Felica@

Delete UMA@

Update ODD schematic for sub board

Add logo board schematic

Remove CIR and LID schematic to sub board

Update TP Button for sub board

Change JHDD1, JHDD2, JUSB, JLVDS, JFP, JFAN, JODD, JIR footprint for ME

Change FAN schematic to PWM

Modify Screw Hole for PHRAA ME

Item	Date	Page	Component	Solution	Request
1)	10/04	44	R290, C309	Reserve RC filter on SPI_CLK	For EMI request
2)	10/04	29	C314	Reserve Reserve 10P Cap on 48MCLK_USB30	For EMI request
3)	10/04	28	C315	Reserve 10P Cap on AZ_BITCLK_HD	For EMI request
4)	10/04	11	C317, C319, C339, C340, C352, C353	Reserve 6PCS 33P cap on +1.5V	For EMI request
5)	10/04	40		LAN_R_GND change to GND	For EMI request
6)	10/04	25	D84	Change P/N and add ESD diode(D84) BOM to SCA00001A00	For ESD request
7)	10/04	38	D82	Change ESD diode (D82) BOM to SC300000100	For ESD request
8)	10/04	37	D85, D86, D87	Reserve ESD diode and close to the connector	For ESD request
9)	10/04	43	DA6, DA7	Change P/N and add ESD diode(D84) BOM to SCA00001A00	For ESD request
10)	10/04	46	D83	Change ESD diode (D83) BOM to SCA00000E00	For ESD request
11)	10/04	32	C516	Reserve C516 on PLT_RST#	For ESD request
12)	10/05	38	JFP	Change footprint to P-TWO_161011-04021	For ME request
13)	10/06	27	L8,L9,L10,L11	Change Common mode choke to SM070000K00	For EMI request
14)	10/06	42	DT2	Change to SC600001600	For ESD request
15)	10/06	42	DT4	Add DT4	For ESD request
16)	10/06	25	R267,R268,R269 R270,R283,R333 R337,R329	Co-lay with optimus support 2-CH panel	For SPEC design ready
17)	10/09	25		Change JLVDS PIN define	For HW4 common design
18)	10/12	25		Change JLVDS PIN define	For layout request
19)	10/12	34	L22,C509	Change to test point T30	On-die VR default support
20)	10/12	34	R483,C280	Change to test point T36	On-die VR default support
21)	10/12	35	R498	Change to test point T41	On-die VR default support
22)	10/12	35	L20,C302	Change to test point T42	On-die VR default support
23)	10/12	35	L17,C296	Change to test point T43	On-die VR default support
24)	10/12	34	R541,R474,R480 R509,R517,R520	Change size to 0402	For layout request
25)	10/12	46		Change LID +3VALW to +3VL	
26)	10/12	06		Change PEG AC coupling caps from 0.22uF to 0.1uF(SE076104K80)	For NVDIA suggest
27)	10/12	13		Change PEG AC coupling caps from 0.22uF to 0.1uF(SE076104K80)	For NVDIA suggest
28)	10/12	09	R122,R252	Change from 100 ohm to 1k ohm	For HW4 schematic review
29)	10/12	09		Add +1.5VS to PJ30 and	For HW4 schematic review
30)	10/12	09		Change +1.5V from PJ30 to Q33	For HW4 schematic review
31)	10/12	29	R564	Change to @	For HW4 schematic review
32)	10/12	33	R124	Delete	For HW4 schematic review
33)	10/12	33	R444	Change BOM structure to mount	For HW4 schematic review
34)	10/12	05		Delete XDP function and change to test point	For layout space
35)	10/12	28		Delete PCH SPI schematic	For layout space
36)	10/12	37		Swap JPIO PIN define	
37)	10/12	42		Swap LT4	For layout request
38)	10/12	05		Update FAN control schematic	For HW4 schematic review
39)	10/12	40	CL43, CL44	Add CL43, CL44	For EMI request
40)	10/12	40	CL683,CL684	Delete CL683,CL684	For layout space
41)	10/12	42	JUSB30	Change to LOTES_AUSB0003-P001C	For ME request
42)	10/14	37	JHDD2	Change to ACES_88058-120N	
43)	10/14	46	H26,H28,H29	Delete	For ME last drawing
44)	10/14	46	H1-H7	Update screw hole	For ME last drawing
45)	10/14	38	L57	Swap L57	For layout request
46)	10/18	37	D86	Swap D86	For layout request
47)	10/18	25	D84	Change D84 BOM structure to install	For ESD request
48)	10/18	43	DA6,DA7	Change DA6,DA7 BOM structure to install	For ESD request
49)	10/18	46	C479,C482,C483 C484,C495,C496 C499,C500,C509 C517,C520	Reserve 0.1u Cap	For ESD request

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title
				<b>SCHEMATIC, MB A7211</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number 4019BD
Date: Monday, February 28, 2011				Sheet 58 of 59

HW PIR (Product Improve Record)

PHRAA LA-7211P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0

GERBER-OUT DATE: 2011/01/31

NO DATE PAGE MODIFICATION LIST

50)	10/20	29	R228	Change R228 from10k to 1k ohm	For Intel spec demand
51)	10/20	41	CC23	Mount CC23	For vendor demand
52)	10/20	44	R172	Change to @ due to the pull high will be in Cap sensor board	
53)	10/20	47	C493	Change C493 from 0.01uF to 0.1uF	To avoid inrush current.
54)	10/25	37	JHDD2	Swap JHDD2	For sub board
55)	10/25	14	RV114,RV115		For NV schematic
56)	10/25	16	RV480,RV481		
57)	10/25	24	RV107,RV109		
			RV116,RV117		
58)	10/26	38	QB4	Change QB4 from SB211970110 to SB00000R300	For sourcer demand
59)	10/26	39	U5	Change U5 from SA000045Z00 to SA00004GV00	For design change
60)	11/12	28	+3V_SPI	Change +3V_SPI to +3VS	For EVT issue
61)	11/12	44	R290	Mount R290	For EVT issue(88)
62)	11/12	11	C317,C319,C339	Mount this part for DDR +1.5V return path	
			C340,C352,C353		
63)	11/12	46	C522-C526	Mount this part	For EMI request
64)	11/12	39	D24	Remove D24	For SUSP# leakage
65)	11/12	20	CV228,CV229	Add VRAM +VRAM_1.5VS power rail	For NV demand
			CV230,CV231		
66)	11/12	21	CV232,CV233	Add VRAM +VRAM_1.5VS power rail	For NV demand
			CV234,CV235		
67)	11/12	22	CV236,CV237	Add VRAM +VRAM_1.5VS power rail	For NV demand
			CV238,CV239		
68)	11/12	44		Change EC GPXI0D04 from SLP_CHG# to OTP_HW	For PWR demand
69)	11/12	44	D26, R359	Add for OTP_HW function	For PWR demand
70)	11/12	44	R1428, R439	Remove for SLP_CHG#	For PWR demand
71)	11/12	26	T75,T76	Add test point at JCRT pin4, pin11	For CIC demand
72)	11/12	39	Q39,Q40	Add Q39,Q40	For avoid SUSP# leakage
73)	11/21	46	JPOWER	Reverse JPOWER pin define	
74)	11/21	37	JHDD2	Reverse (vertical and horizontal) JHDD2 pin define	
75)	11/21	46	H8,H9	Change H8&H9 to 3P3	
76)	11/25	42	LT1,LT2	Change to SM070001U00	For EMI request
77)	11/25	40	CL37,CL38	Remove CL37 and change CL38 from 4.7U to 220P	For EMI request
78)	11/25	40	LL4-LL11	Reserve LL4-LL11	For EMI request
79)	11/25	44	R383	Delete R383	For HW4 LID SW common design
80)	11/25	25,43	C13,CA28	Add C13 and CA28	For EMI request
81)	11/25	38		Seap JIR PIN define	For common with PHQAA
82)	11/25	46	C484,C495,C527	Reserve 0.1u Cap	For ESD request
83)	11/25	40	CL484-CL487	Add CL484-CL487 to 0.1 cap	For EMI request
84)	12/28	42	UT1	Change P/N to SA000048H00	
85)	12/28	25	R131	Add R131 for Sumsong panel issue	For panel issue
86)	12/28	44	R383	Add R383	For HW4 LID SW common design
87)	12/28	35	C333,C515	Change C333, C515 to 10uF	For HW4 cost down plan
88)	12/28	37	C426	Change C426 BOM structure to @	For HW4 cost down plan
89)	12/28	44	R398,U44,C818	Add R398 and change U44,C818 BOM structure to @	For HW4 cost down plan
90)	12/29	35	L19,L21	Change L19,L21 to SM010028480	
91)	12/29	37	C375-C378	Add C375-C378 on ODD fuction	For HW4 cost down plan
92)	12/29	37	C360	Add C360	For ESD request
93)	12/29	44	R475,R738,R739	Add R475,R738,R739	For 9012 co-lay
94)	01/19			Change D9,D55,DG1,D7,D8,D12,D14,D16,D21,D26, D25 to SCS00000200	
95)	01/19	05	D88	Change D88 to SC100001M00	
96)	01/19			Change U2 P/N to SA00004EE80	
97)	01/19	25	R387	Change R387 BOM structure to @	For 3D panel brightness issue
98)	01/19	08	C890,C894	Delete C890, C894	For power request
99)	01/19	08	C890	Change C891 to SGA20331E10	For power request
100)	01/19	08	C2,C7	Add C2,C7	For power request
101)	01/19	09		Change C873 to C112	For low ESR to pass transi
102)	01/19	25	R131	Change R131 to 47K	For 3D panel brightness issue
103)	01/19	32	R399	Change R399 BOM structure to @	For optimus device loss issue
104)	01/19	32	R544	Change R544 BOM structure to OPT@	For optimus device loss issue
105)	01/19	47	R434	Change R434 from 47K to 220K	For optimus device loss issue
106)	02/10	09	R877	Change R877 to @	For VCCSA voltage margin check
107)	02/10	32	R360	Add R360 to 0.1u	For ESD request
108)	02/10	46	U2	Change U2 P/N to SA00004EET0(R3 P/N) and SA00004EES0(R1 P/N)	
109)	02/10	46	UV1	Change UV1 P/N to SA000047U00(R3 P/N) and SA000047U20(R1 P/N)	
110)	02/10	46	PCB	Change PCB P/N to DAZ01700100	